



A Subthreshold Biased CMOS Ring Oscillator Model Design in 180-nm Process

Vinícius Henrique Geraldo Correa, Rodrigo Aparecido da Silva Braga*,
Dean Bicudo Karolak & Fernanda Rodrigues Silva

Institute of Sciences and Technology, Federal University of Itajuba – Campus Itabira,
Itabira-MG, 35903087, Brazil

*E-mail: rodrigobraga@unifei.edu.br

Abstract. In this paper, a 180-nm CMOS ring oscillator design, made with halo-implanted transistors and operating in the weak inversion region, is proposed, based on an undergraduate integrated circuit design course methodology for building logic gates and comparing simulated results with reviewed literature data. Halo-implanted channel transistors have a steeper and less distorted voltage characteristic curve compared to uniformly doped channel ones, which makes them a more appropriate option when designing asynchronous digital integrated circuits aimed at low bias and low power. Three gate models were created using weak inversion and pull-up and pull-down networks made with halo-implanted transistors. The results of the study and simulation of the three inverter digital gate topologies showed that the NOT inverter model, as expected, had a higher frequency than the NAND and NOR inverter models. The ring oscillators made with the NOT inverter came up with an 8.25-MHz switching frequency as well as a dynamic power close to 270 nW. A comparison with other ring oscillators from previous studies is also shown.

Keywords: CMOS; halo-implanted channels; low-power integrated circuits; ring oscillators; weak inversion operation.

1 Introduction

Digital circuit designs at the nanoscale dimension face trade-offs between speed operation, energy consumption, size, and applicability [1]. A CMOS ring oscillator is a circuit that can be designed by cascading logic inverters or differential pairs in a loop, with the first option having better frequency performance, as shown by Bin Mohd Mokhtar, *et al.* in [2]. Although normally done with an odd number of stages, Fahs, *et al.* in [3] proposed a two-stage ring oscillator made with differential pairs; Razavi in [4] proposed a single-stage BicMOS oscillator; Djahanshahi in [5] designed a robust one-stage InP – HBT oscillator. In addition, different bias values can be applied to the substrate, obtaining different results; Nyathi and Bero in [6] showed several substrate bias techniques, resulting in shorter propagation delays for logic gates compared to

Received July 15th, 2021, 1st Revision February 7th, 2023, 2nd Revision April 4th, 2023, Accepted for publication June 16th, 2023.

Copyright © 2023 Published by IRCS-ITB, ISSN: 2337-5787, DOI: 10.5614/itbj.ict.res.appl.2023.17.2.1

the traditional biasing method, however, the use of NAND, NOR and XNOR gates as inverters is not addressed in this work.

The works presented in [15-16] show the effect of a low supply voltage on the voltage transfer characteristic curve (VTC) of CMOS inverter circuits. For supply voltage values below 0.1 V, the VTC presents distortions on it. Alioto in [16] associated this behavior with the leakage current, stating that in a weak inversion region, this current cannot be neglected in relation to the total circuit current flow. Therefore, the choice of the supply voltage of the project is very important; besides, the lower the supply voltage, the bigger the propagation delay, as found by Kitchener in [13].

Halo implants in transistors' channels cause shifts in the threshold voltage (V_{TH}) [14] and also anomalies in the transconductance, as shown by Agarwal, *et al.* in [26]. These characteristics must be considered in circuit designs in the weak inversion region, as this type of technology can be used to reduce short channel effects, as stated by Roy, *et al.* in [14]. A ring oscillator circuit can be used on clock pulse generators and thermic devices for various classes of SoCs, such as FPGAs and microcontrollers [7-12], allowing designs on digital signal processing systems and low power controllers. However, these low-power circuits face problems in the output frequency due to propagation delay, as depicted by Kitchener in [13], leading to very low frequency values compared to the strong inversion biased ones.

In this paper, we present the design of a ring oscillator that operates in the region of weak inversion. First, we investigated the voltage transfer characteristics of uniformly doped and halo-implanted channels CMOS inverters, evaluating the logic switching behavior as well as the noise margins of different types of inverter logic gates. Subsequently, we will discuss the analysis of three topologies for a ring oscillator design, using NOT inverters, NAND and NOR gates, respectively. Niiyama, *et al.* in [17] used two and three terminal NAND gates as inverters in their design.

Walunj, *et al.* in [18] presented a weak inversion CMOS ring oscillator using smaller dimensions compared to the ones proposed in the present work, but they did not give the details of its technology channel. The three-stage inverter ring oscillator implemented with halo-implanted channel transistors on weak inversion operating on a supply voltage of 400 mV showed the best performance. This approach achieved a frequency value of 8.25 MHz as well as less delay in signal propagation and dynamic power close to 270 nW.

This article is structured as follows. In Section 2, we characterize the behavior of CMOS circuits in weak inversion as well as the characteristics of the technology

used for the project. Next, in Section 3, we describe the steps used to design a halo-implanted channel CMOS inverter, contrasting its behavior with that of the uniformly doped channel inverter.

In Section 4, we present the design of the NAND and NOR logic gates by means of pull-up (PUN) and pull-down (PDN) networks in order to support the study of other inverter topologies. In Section 5, we show the design and analysis of three ring oscillator topologies using three different logic gates. Finally, in the conclusion section we guide the scope of the study and provide the conclusions in light of the presented data.

1.1 Digital Integrated CMOS Circuits Operating in Weak Inversion

The manipulation of a field effect transistor, in order to set it as a signal amplifier or digital switch, is achieved by biasing the voltages in the drain, source, gate and substrate terminals. To operate as a switch, the cut-off and triode regions define the high and low logic levels at the output. Thus, when the transistor's gate has a low logic level, it behaves like an open logic switch, preventing the flow of charges between the drain and source terminals. Otherwise, if a high logic level is applied to the gate, the device's characteristic behavior is located in the triode region, allowing maximum current to flow through it, which makes it function as a closed logic switch.

The weak inversion operation point is achieved when the DC voltage bias between the gate and source (V_{GS}) of a MOS transistor is kept below the threshold voltage [19], which contrasts with the bias values in strong inversion. In weak inversion, most of the charge flow through source and drain comes from the diffusion current, as described by Vittoz and Fellrath in [20].

The behavior of the drain-source current (I_{DS}) of a MOS transistor in weak inversion is given by Eq. (1), where K is the Boltzmann constant; T is the temperature, in Kelvin; q is the elementary charge in Coulomb; n and I_s are technology-based parameters [21]:

$$I_{DS} = I_s \left(\frac{W}{L} \right) \exp \left(\frac{q(V_{GS} - V_{TH})}{nkT} \right) \left[1 - \exp \left(- \frac{qV_{DS}}{kT} \right) \right] \quad (1)$$

To carry out this project, we used 180-nm TSMC technology under the Synopsys software for creating and editing schematics and layouts of integrated circuits, focusing on a voltage range that guarantees operation in the weak inversion region and a steep voltage transfer curve for better performance in logic switching.

2 Methodology

2.1 Project and Characterization of a CMOS Inverter in Weak Inversion

The working principle of the CMOS inverter, shown in Figure 1, consists of the alternation between the cut-off and triode states of the complementary transistors, controlled by the input voltage (v_{in}).

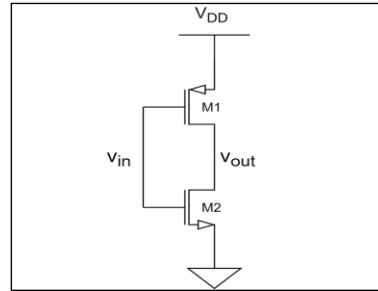


Figure 1 Typical schematic of a CMOS inverter circuit.

In order to evaluate the effects of the channel type on the inverter, we compared two technologies. Figure 2(a) shows the VTC of the halo-implanted and the uniformly doped long channel inverters under testing. Tables 1 and 2 show their contrasts based on the threshold and dimension values.

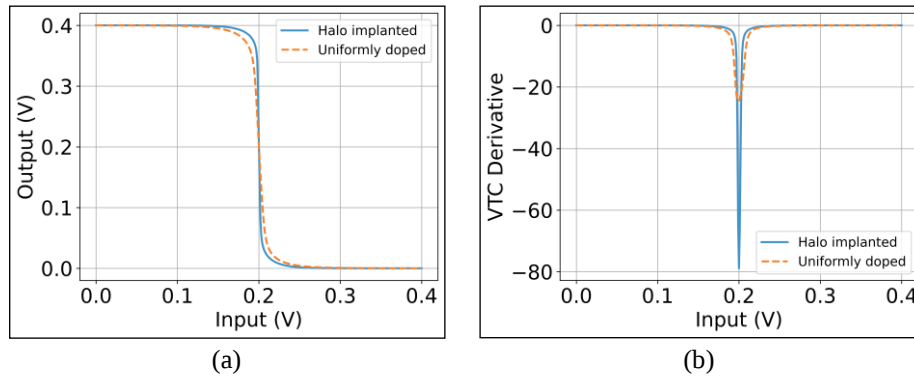


Figure 2 (a) VTC of halo-implanted and uniformly doped inverters. (b) Slopes of the VTCs of the halo-implanted and the uniformly doped channel inverter.

The higher current and higher transconductance and gain behavior displayed by the halo-implanted transistor [22] leads its inverters to a more pronounced response in the voltage transfer characteristic, as shown in Figure 2(a). This tends

to offer a slightly higher noise margin, as can be seen in Table 3, where the data are close to those presented by Kitchener in [13].

Table 1 Halo-implanted and uniformly doped channel inverter transistor operating under 0.4 V on V_{DD} .

	Halo-implanted	Uniformly doped
W_p [μm]	5.87	1.36
W_n [μm]	2.00	2.00
L_p [nm]	350	350
L_n [nm]	350	350

Table 2 Electrical characteristics of the pMOS and nMOS transistors for the halo-implanted and uniformly doped channel inverters operating under 0.4 V on V_{DD} .

	Halo-implanted	Uniformly doped
V_{THn} [V]	0.531	0.742
V_{THp} [V]	-0.538	-0.843
g_{mn} @ V_{SP} [nS]	35.72	40.76
g_{mp} @ V_{SP} [nS]	36.07	42.43
I_{DSn} @ V_{SP} [nA]	1.26	1.60
I_{DSp} @ V_{SP} [nA]	-1.26	-1.60

Therefore, when the gate voltages of both transistors have a value of 0 V, the pMOS is ideally located in the triode region, functioning as a low-resistance path, and the nMOS is in the cut-off region (open switch). Thus, at the output we have a high logic level. Otherwise, in the presence of a high logic level (V_{DD}) at the input, the opposite will occur, since the nMOS would be in the triode region and the pMOS in the cut-off region, so we will have a low logic output voltage level (GND). In the transition region between inverter states, where the input voltage level is close to half the supply voltage, we have both transistors in saturation, which gives the output a voltage close to $V_{DD}/2$ in case of matched nMOS and pMOS. The faster the response of the state transition curve, the closer the inverter gets to the ideal.

The VTC derivatives of the inverters, as shown in Figure 2(b), lead us to verify that the halo-implanted one shows a higher gain due to the anomalous behaviors in the transconductance induced by the halo-implanted pockets [26], as observed by the slope in the switching point voltage (V_{SP}) region, which confirms the steeper behavior in the transition between logic states for the halo-implanted technology. Using the two point values where the slope is equal to -1 (see Figure 2(b)), we evaluated V_{IL} , V_{IH} , V_{OL} , and V_{OH} of the two channel technologies, enabling the calculation of their noise margins, as shown in Table 3. Noting that the halo-implanted inverter showed higher noise margins and better VTC, we

chose its channel technology to lead our entire project. These noise margins values were calculated by Eqs. (2) and (3) [23]:

$$NM_H = V_{OH} - V_{IH} \quad (2)$$

$$NM_L = V_{IL} - V_{OL} \quad (3)$$

Table 3 Voltage values and noise margins of the halo-implanted and the uniformly doped inverter.

	Halo-implanted	Uniformly doped
V_{DD} [mV]	400 mV	400 mV
V_{IL}	186 mV	178 mV
V_{IH}	216 mV	222 mV
V_{OL}	13.7 mV	16.4 mV
V_{OH}	386 mV	381 mV
NM_H	170 mV	159 mV
NM_L	172.3 mV	161.6 mV

Continuing the study, we performed an analysis of the supply voltages in the halo-implanted inverter in order to verify the degradation behavior on the voltage transfer curves for different values of V_{DD} . The result of this analysis, shown in Figure 3, show similar behavior as that presented in [15] and [16], thus we can see that even with a higher noise margin, the VTC degradation for low voltage supplies also occurs in halo-implanted transistors.

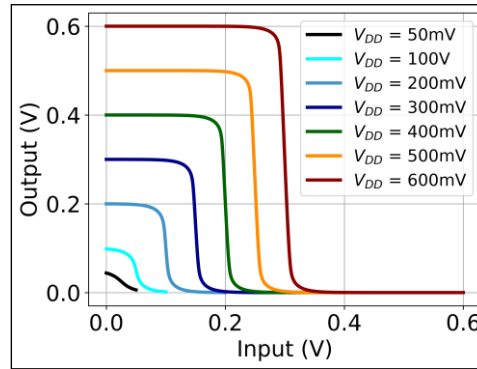


Figure 3 VTC for several supply voltages in the halo-implanted transistor.

2.2 Design and Characterization of NAND and NOR Gates in Weak Inversion

In order to verify the behavior of the halo-implanted VTC for different models, we also studied two other inverter configurations, using NAND and NOR logic gates, respectively. To achieve the low voltage for the weak inversion region, a

smaller propagation delay, and minimum distortion in the characteristic curve of the project, we set 400 mV as supply voltage.

By using the same 180-nm TSCM technology as presented by Kitchener in [13], but with a temperature of 25 °C, we designed the aspect ratio such that voltage V_{DS} is equivalent to $V_{DD}/2$ for each transistor of the CMOS inverter (see Table 4). For the logic gates, the sizing conventions of PUN and PDN networks were used [23]. Thus, the channel widths of the transistors for NAND's PDN network and NOR's PUN network were doubled, as also depicted in Table 4.

Figure 4 shows the PDN and PUN networks that we used in this project, and Figure 5 shows a symbolic representation of the configuration of the logic gates as inverter circuits.

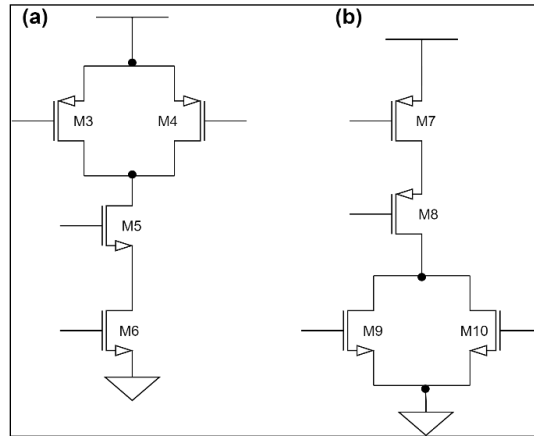


Figure 4 (a) PUN and PDN networks for the NAND logic gate. (b) PUN and PDN networks for the NOR logic gate.

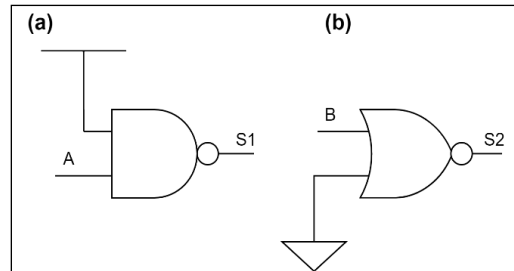


Figure 5 Typical schematic of a CMOS inverter circuit.

Table 4 shows the resulted current I_{DS} , V_{DS} , V_{TH} , and the aspect ratio for the three proposed transistors with 400 mV as voltage supply.

Table 4 Bias and dimension values of the NOT's PDN and PUN transistors in Figures 1, 4(a) and 4(b) for $V_{DD} = 0.4$ V.

	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
I_{DS} [nA]	-2.20	2.20	-0.20	-0.20	0.41	0.41	-0.43	-0.43	0.21	0.21
V_{DS} [V]	-0.19	0.200	-0.117	-0.117	0.159	0.123	-0.118	-0.159	0.121	0.121
V_{TH} [V]	-0.58	0.555	-0.588	-0.588	0.593	0.559	-0.590	-0.627	0.557	0.557
W [μ m]	6.19	2.00	6.19	6.19	4.00	4.00	12.38	12.38	2.00	2.00
L [nm]	180	180	180	180	180	180	180	180	180	180

The switching behavior of the inverters is shown in Figure 6(a). By deriving these VTCs, as can be seen in Figure 6(b), we see that although the NOT inverter's switching point voltage was the most balanced, at $V_{DD}/2$ its transition was the least steep. The most expressive transition was observed in the NAND inverter. The values of low and high input and output voltages (V_{IL} , V_{IH} , V_{OL} and V_{OH}) as well as the noise margins of the three inverters are shown in Table 5.

Table 5 Inverters' voltages and noise margins.

	NOT	NAND	NOR
V_{IL} [mV]	181	174	194
V_{IH} [mV]	221	210	230
V_{OL} [mV]	13.8	14.4	13.7
V_{OH} [mV]	385	385	384
NM_H [mV]	164	175	154
NM_L [mV]	167	159	180

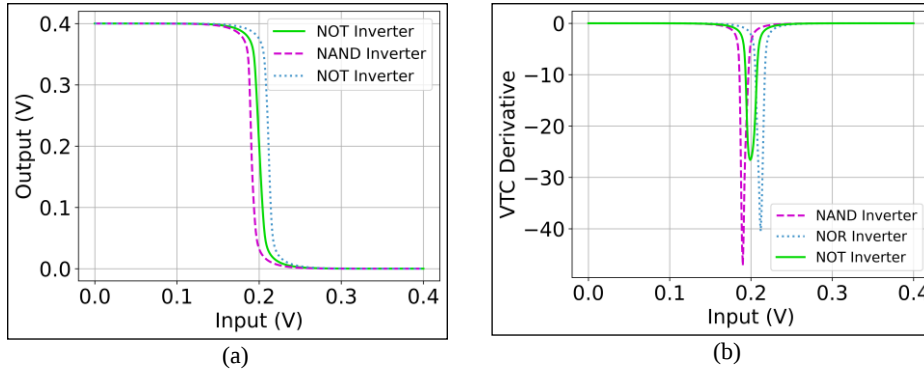
**Figure 6** (a) VTC of the three inverter gates, for $V_{DD} = 400$ mV. (b) VTC's slopes of the three inverter gates.

Table 6 presents the t_{PHL} , t_{PLH} and the average propagation delay (τ) of the three logic gates. The values are in line with those presented by Kitchener in [13], where τ is obtained by the arithmetic mean of the ascent and descent times [23].

Table 6 t_{PHL} , t_{PLH} and propagation delay for the logic gates with $V_{DD} = 0.4V$.

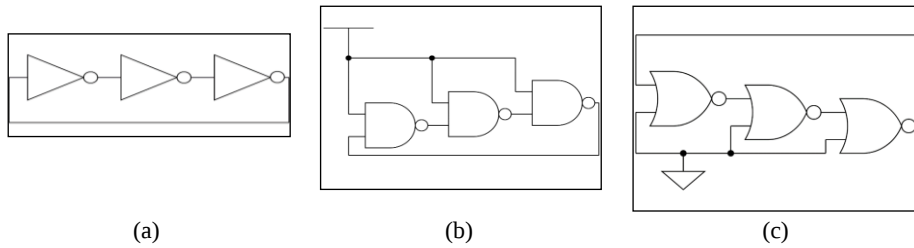
	NOT	NAND	NOR
t_{PHL} [ns]	788	795	787
t_{PLH} [ns]	725	803	739
τ [ns]	756	799	763

2.3 Design and Characterization of a Ring Oscillator Operating in Weak Inversion

In this work, we chose the design of a ring oscillator circuit formed by cascading inverting logic gates. Thus, due to the delayed response of the gates, the oscillation cycle allows periodic variation of the voltage at the output of each inverter, which feeds the other component gate of the cycle, maintaining a constant oscillation of the output voltage level, as expected [23].

The output frequency of a CMOS ring oscillator built with NOT inverters is given by $f = 1/2N\tau$ [23], where N is the number of gates and τ is the propagation delay. Thus, it is observed that the frequency depends on the propagation delay and the number of cascading logic gates. A high number of stages would result in a lower output frequency; therefore, a low number of logic gates should be a key point of focus in the development of a ring oscillator.

Aiming for a smaller number of stages in the oscillator in order to guarantee a high frequency, we designed three ring oscillators with the topologies presented in the schematic circuits of Figures 1 and 5, with three cascading logic gates, as shown in Figure 7.

**Figure 7** (a) NOR, (b) NAND and (c) NOR ring oscillator circuits.

The output behavior of the three oscillators is shown in Figure 8(a) and the dynamic behavior is described in Table 7. Table 7 shows the t_{PLH} , t_{PHL} , and propagation delay for the ring oscillators, again showing lower switching time values for the NOT gate devices. To verify the frequency behavior of the three ring oscillators, we conducted a simulation regarding frequencies t_{PHL} and t_{PLH} for several numbers of stages. Figure 8(b) shows how the oscillators' frequencies behave when increasing the number of gates.

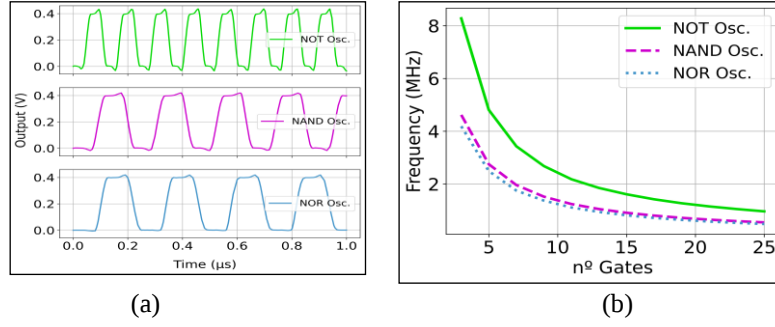


Figure 8 (a) Output of the NOT, NAND and NOR ring oscillators. (b) Frequency per number of gates for the NOT, NAND and NOR ring oscillators.

Table 7 Dynamic behavior of the three-stage ring oscillators.

	NOT Osc.	NAND Osc.	NOR Osc.
$t_{PHL}[\text{ns}]$	22.5	37.1	32.4
$t_{PLH}[\text{ns}]$	19.9	31.9	35.9
$\tau[\text{ns}]$	21.2	34.5	34.15
Period [ns]	121	217	239

The NOT inverter ring oscillator had the highest frequency values, and also the lowest t_{PHL} , t_{PLH} and propagation delay, as shown in Figures 9(a) and 9(b), because of which it is considered the best topology for the project.

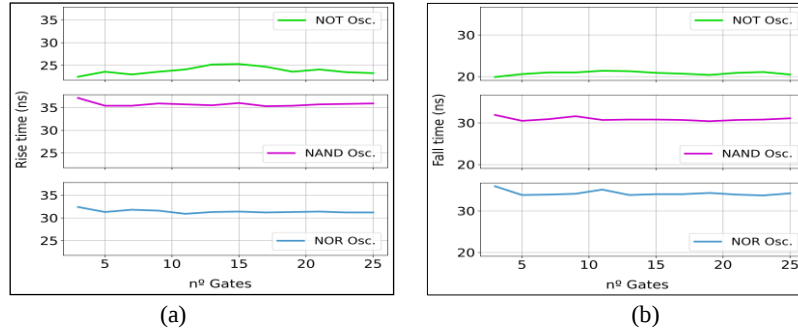


Figure 9 (a) Rise time comparison per number of gates for the NOT, NAND and NOR ring oscillators. (b) Fall time comparison per number of gates for the NOT, NAND and NOR ring oscillators.

Although it produces a lower frequency, the weak inversion ring oscillator compensates this by reducing the power, as $P = fC(V_{DD})^2$ [23], where C stands for the total capacitance of the circuit. The power–delay product can be estimated by $PDP = P/2Nf$. One can notice that by reducing V_{DD} and the frequency, the circuit will come up with lower power values and thus lower energy consumption.

Table 8 shows a comparison of our results with other CMOS ring oscillators. Walunj, *et al.* in [18] reported a higher frequency than our work but with a smaller dimension and a lower bias in its work, which makes us consider using smaller dimensions along with weak inversion to achieve better results in terms of frequency and power. By contrast, [24-25] proposed 180-nm ring oscillators made with differential pairs stages in the strong inversion region, resulting in higher frequencies and higher power consumption, as expected.

Table 8 Comparison of results with other works.

	[24] 2011	[25] 2016	[18] 2018	Proposed
Technology	180 nm	180 nm	32 nm	180 nm
Model type	Diff. Pair	Diff. Pair	NOT Inv.	NOT Inv.
N° of Stages	3	2	5	3
V _{DD}	1.0 V	1.8 V	0.3 V	0.4 V
Frequency	4090 MHz	4000 MHz	66 MHz	8.25 MHz
Power	13000 μ W	11060 μ W	0.257 μ W	0.27 μ W
PDP	530 fJ	691 fJ	0.389 fJ	5.45 fJ

Finally, we show the layout of the NOT ring oscillator circuit. Figure 10 shows the design. The layout was built to be simple and with a small surface area, in order to produce a compact circuit model, reduce the costs, and also minimize the capacitance effects produced by the metal connections and other materials, resulting in an area of 358 μm^2 .

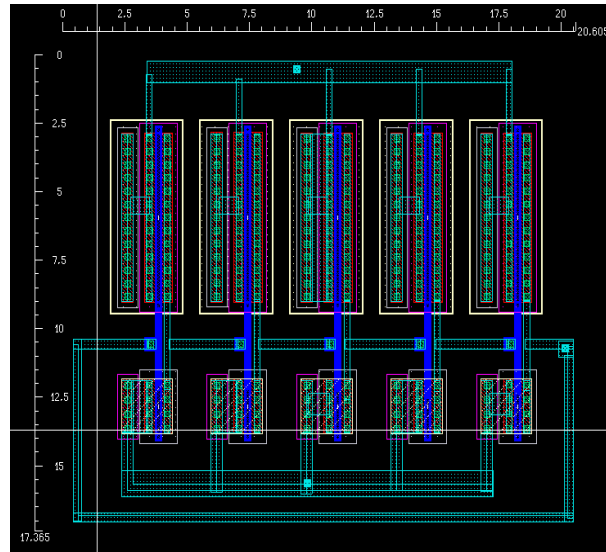


Figure 10 Proposed layout for a five-stage NOT ring oscillator circuit model, with a width of about 20.605 μm and a length of 17.365 μm for the entire ring oscillator area.

3 Discussion

In summary, we began the designing our model by performing an analysis of the channel type of the circuits that would be used for the construction of the ring oscillator, comparing VTC behaviors for the uniformly doped and halo-implanted channel technologies. Regarding the anomalous transconductance behaviors due to halo pockets in the channel [26], we observed that the halo-implanted transistors showed a steep curve, so we decided to choose this technology for our design. We then verified the behavior of the halo-implanted channels for different voltage values. Then we built a basic CMOS inverter with an NMOS transistor and another PMOS, analyzing the characteristic curves for the circuit under 0.4 V of source supply.

To verify the behavior of other logic gates, we analyzed NAND and NOR inverters, also with the halo-implanted transistors technology. Considering that the NOT gate showed lower switching time values, we decided to choose this logic gate as the best stage to build our ring oscillator model. To decide the number of stages used in the project, we also checked the behavior of frequency, t_{PHL} , t_{PLH} , and propagation delay for the three ring oscillators models by varying the number of stages and comparing their performances.

Finally, we performed an analysis of the power and PDP for the NOT ring oscillator, comparing our results with previous studies. Our proposed three-stage ring oscillator, biased for the weak inversion region of operation showed 8.25 MHz in frequency, which is much lower than the 4090 MHz of the three-stage difference pair ring oscillator presented in [24], which was built with the same 180-nm channel dimension and under 1.0 V of source supply. Walunj *et al.* [18], also using a subthreshold bias approach and simulations, came with a five-stage NOT inverter ring oscillator with 66 MHz, but it was built with smaller dimensions and a different technology. As a trade-off, in terms of power, our model showed a similar value as that presented in [18], which is lower than that presented in [24].

Figure 11 shows a flowchart resuming the design process in this work in five steps. The presented design can be used to develop other advanced projects, or even come up with another approach for building this kind of circuitry.

The project design presented in this work was shown to be a useful benchmark for future asynchronous digital integrated circuits biased for weak inversion, and also a helpful tool for test benches on simulated and physical analysis regarding halo-implanted technologies, number of stages, terminal voltages, and dimensions.

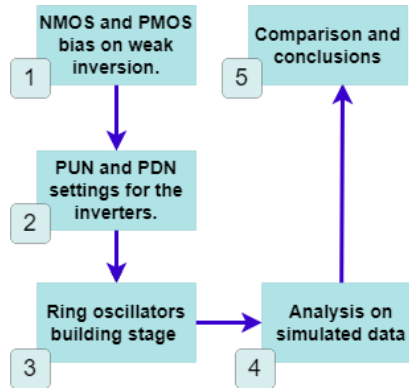


Figure 11 Flowchart depicting the steps involved in designing the presented ring oscillator model.

4 Conclusion

Design frameworks for integrated circuits vary from project to project. The formula presented in this study shows a simple and effective pipeline for building, testing, and analyzing CMOS ring oscillators. In this paper, we presented a halo-implanted channel CMOS ring oscillator model, biased for the weak inversion operation region, with a focus on low power consumption. The results showed that halo implants provide better behavior in terms of switching characteristics of the inverter gate due to the higher transconductance and gain, producing a greater noise margin in contrast with the other ones made with uniformly doped long channels. The behavior of the three inverter gates studied leads us to conclude that the NOT gate is the most appropriate one to be used in ring oscillators, and three cascaded stages will give it a frequency of 8.25 Mhz and a power value close to 0.27 uW, allowing applications with low voltage supply, frequency, and power.

Limitations and future work

The data presented in this work come from simulated analysis, made by software that generally has some contrast and measurement errors related to the real behavior of a physical device. Therefore, in future works one can use the framework shown here to build experimental ring oscillators with three or more extra stages to analyze the performance of a NOT ring oscillator along with other technologies and different projects, such as digital controllers, signal processing devices and FPGAs. We also have some works related to the proposed layout, so a keen analysis of the dimensions of the connections and the layout model may help to come up with a fast switching response or lower power consumption.

Acknowledgment

This work was supported by the Institute of Sciences and Technology (ICT), Federal University of Itajubá, Campus Itabira through funding under the Institutional Scientific Initiation Scholarship Program.

References

- [1] Croon, J.A., Sansen, W.M. & Maes, H.E., *Matching Properties of Deep Sub-Micron MOS Transistors*. Springer, 2005.
- [2] Bin Mohd Mokhtar, H., Bin Zoolfakar, A.S. & Binti Hashim, H., *Comparison between Inverter and Differential Amplifier as 0.35 μ m Ring Oscillator Vehicle*, in 2008 IEEE Conference on Innovative Technologies in Intelligent Systems and Industrial Applications, IEEE, pp. 116–118, 2008.
- [3] Fahs, B., Ali-Ahmad, W.Y. & Gamand, P., *A Two-Stage Ring Oscillator in 0.13-Mm CMOS for UWB Impulse Radio*, IEEE Transactions on Microwave Theory and Techniques, **57**(5), pp. 1074-1082, 2009.
- [4] Razavi, B., *A 2-GHz 1.6-mW Phase-locked loop*, IEEE Journal of Solid-State Circuits, **32**(5), pp. 730-735, 1997.
- [5] Djahanshahi, H., Saniei, N., Voinigescu, S.P., Malikpaard, M. & Salama, C.A.T., *A 20-GHz INP-HBT Voltage-Controlled Oscillator with Wide Frequency Tuning range*, IEEE Transactions on Microwave Theory and Techniques, **49**(9), pp. 1566-1572, 2001.
- [6] Nyathi, J. & Bero, B., *Logic Circuits Operating in Subthreshold Voltages*, in Proceedings of the 2006 International Symposium on Low Power Electronics and Design, pp. 131-134, 2006.
- [7] Kodýtek, F. & Lórencz, R., *A Design of Ring Oscillator Based PUF on FPGA*, in 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems. IEEE, pp. 37-42, 2015.
- [8] Franco, J.J.L., Boemo, E., Castillo, E. & Parrilla, L., *Ring Oscillators as Thermal Sensors in FPGAs: Experiments in Low Voltage*, in 2010 VI Southern Programmable Logic Conference (SPL), IEEE, pp. 133-137, 2010.
- [9] Gag, M., Wegner T., Waschki, A. & Timmermann, D., *Temperature and On-Chip Crosstalk Measurement Using Ring Oscillators in FPGA*, in 2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS). IEEE, pp. 201-204, 2012.
- [10] Pons M., Müller, C.T., Ruffieux, D., Nagel, J.L., Emery, S., Burg, A., Tanahashi, S., Tanaka, Y. & Takeuchi, A., *A 0.5 v 2.5 μ W/MHz Micro-Controller with Analog-Assisted Adaptive Body Bias PVT Compensation with 3.13 Nw/Kb SRAM Retention in 55nm Deeply-depleted Channel*

- CMOS, in 2019 IEEE Custom Integrated Circuits Conference (CICC). IEEE, pp. 1-4, 2019.
- [11] Coustans, M., Krummenacher, F., Kayal, M. & Terrier, C., *A nA Crystal-Less Oscillator for Internet of Things*, in 2016 MIXDES – 23rd International Conference Mixed Design of Integrated Circuits and Systems, IEEE, pp. 136-139, 2016.
 - [12] Labbé, B., Fan, P., Achuthan, T., Prabhat, P., Knight, G.P. & Myers, J., *A Supply Voltage Control Method for Performance Guaranteed Ultra-Low-Power Microcontroller*, IEEE Journal of Solid-State Circuits, 2020.
 - [13] Kitchener, J.A., *Subthreshold and Near-threshold Techniques for Ultra-low Power CMOS Design*, PhD Dissertation, School of Electrical and Electronic Engineering, Faculty of Engineering, Computer and Mathematical Sciences, The University of Adelaide, Adelaide, 2015.
 - [14] Roy, A.S., Mudanai, S.P. & Stettler, M., *Mechanism of Long-channel Drain-induced Barrier Lowering in Halo MOSFETs*, IEEE Transactions Devices, **58**(4), pp. 979-984, 2011.
 - [15] Swanson, R.M. & Meindl, J.D., *Ion-Implanted Complementary MOS Transistors in Low-Voltage Circuits*, IEEE Journal of Solid-State Circuits, **7**(2), pp. 146-153, 1972.
 - [16] Alioto, M., *Understanding DC Behavior of Subthreshold CMOS Logic Through Closed-Form Analysis*, IEEE Transactions on Circuits and Systems I: Regular Papers, **57**(7), pp. 1597-1607, 2010.
 - [17] Niiyama, T., Piao, Z., Ishida, K., Murakata, M., Takamiya, M. & Sakurai, T., *Increasing Minimum Operating Voltage (VDDmin) with Number of CMOS Logic Gates and Experimental Verification with Up to 1 Mega-Stage Ring Oscillators*, in Proceedings of the 2008 International Symposium on Low Power Electronics & Design, pp. 117-122, 2008.
 - [18] Walunj, R.A., Pable, S.D. & Kharate, G.K., *Design of Robust Ultra-low Power CMOS Voltage Controlled Ring Oscillator with Enhanced Performance*, in 2018 International Conference on Advances in Communication and Computing Technology (ICACCT), IEEE, pp. 235-239, 2018.
 - [19] Tsividis, Y. & McAndrew, C., *Operation and Modeling of the MOS Transistor*, Oxford Univ. Press, 2011.
 - [20] Vittoz, E. & Fellrath, J., *CMOS Analog Integrated Circuits Based on Weak Inversion Operations*, IEEE Journal of Solid-State Vircuits, **12**(3), pp. 224-231, 1977.
 - [21] Ferreira, L.H. & Sonkusale, S.R., *A 60-Db gain OTA operating at 0.25-V power supply in 130-nm digital CMOS process*, IEEE Transactions on Circuits and Systems I: Regular Papers, **61**(6), pp. 1609-1617, 2014.
 - [22] Braga, R.A., Ferreira, L.H., Coletta, G.D. & Dutra, O.O., *A 0.25-v Calibration-Less Inverter-Based OTA for Low-Frequency Gm-C Applications*, Microelectronics Journal, **83**, pp. 62-72, 2019.

- [23] Sedra, A. & Smith, K., *Microelectronic Circuits*, ed. 7, Oxford University Press, 2015.
- [24] Sheu, M.-L., Tiao, Y.-S. & Taso, L.-J., *A 1-V 4-GHz Wide Tuning Range Voltage-Controlled Ring Oscillator in 0.18 μ m CMOS*, *Microelectronics Journal*, **42**(6), pp. 897-902, 2011.
- [25] Gargouri, N., Sakka, Z., Issa, D. B., Kachouri, A. & Samet M., *A 4GHz Temperature Compensated CMOS Ring Oscillator for Impulse Radio UWB*, in 2016 7th International Conference on Sciences of Electronics, Technologies of Information and Telecommunications (SETIT), IEEE, pp. 71-75, 2016.
- [26] Agarwal, H., Gupta, C., Dey, S., Khandelwal, S., Hu, C. & Chauhan, Y. S., *Anomalous Transconductance in Long Channel Halo Implanted MOSFETs: Analysis and Modeling*, *IEEE Transactions on Electron Devices*, **64**(2), pp. 376-383, 2017.