Performance Evaluation of Nanoscale Single- and Dual-Gate MESFETs Using COMSOL Multiphysics

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Abstract. In this work, a comparative numerical simulation of single-gate and double-gate depletion mode GaAs MESFETs in the nanometer domain using COMSOL Multiphysics was carried out. The objective was to evaluate the significance of multi-gate structures based on electrostatic control capability in terms of performance improvement in Schottky gate MESFETs. Four models were considered, including a traditional single-gate model, an analogous double-gate model, and their corresponding reduced scale models. Comparisons were made in terms of the concentration of electrons and output response depending on the value of the gate bias voltage. There were almost no differences between the two models when scaled at the same dimensions. The reduced dual-gate device exhibited lower leakage current and superior channel control compared to its single-gate counterpart, particularly with higher drain bias applied. This suggests that while the dual-gate design may not be advantageous in all dimensions, it proves more effective when MESFET structures are aggressively scaled, indicating that dual-gate configurations are preferable for nanoscale GaAs MESFETs operating in regimes where electrostatic degradation is significant.

Keywords: *COMSOL Multiphysics; dual-gate MESFET; electrostatic control; GaAs MESFET; leakage current; nanoscale transistor.*

1 Introduction

The metal-semiconductor field-effect transistor (MESFET) is a significant device in high-frequency applications, as the Schottky gate provides fast control of the channel without the need for a p-n gate junction [1, 2]. In gallium arsenide (GaAs) technology, MESFETs have traditionally been linked with microwave and high-speed applications owing to the transport characteristics of the semiconductor and the suitability of Schottky-gated devices for high-frequency operation [3]. Although new families of transistors, such as the high-electron-mobility transistor (HEMT) and multigate metal–oxide–semiconductor field-effect transistors (MOSFETs), are now the dominant devices in leading-edge applications [4], the MESFET is a valuable device for understanding the mechanisms of field control [1], scaling, and the relationship between device geometry and electrostatics in the channel region [5].

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As the dimensions approach the nanoscale region, the performance of a conventional single-gate device becomes very sensitive to the effects of electrostatic degradation [6, 7]. The control over the channel becomes weaker, the effects of leakage are felt, and the drain field starts affecting the conducting region [8]. In the context of broad transistor design, the concept of multi-gate devices is introduced to solve this problem by enhancing the electrostatic coupling between the gate and the channel [9, 10]. This concept is well established in the context of scaled transistors, where the control over the channel is maximized to reduce the effects of leakage [11, 12].

This premise motivated the present study. Rather than assuming the superiority of the dual-gate configuration a priori, this work evaluated its performance systematically through simulation. A previously existing nanoscale depletion-mode MESFET model was used as the basis for this work [13]. A second device was created that was identical in terms of dimensions to the original device but with a dual-gate structure [14]. This was done so that the effect of gate structure could be isolated [15]. This same methodology was used for reduced dimension devices in order to assess whether dimensional scaling affects single-gate versus dual-gate structures.

The main contribution of this work is the scale-dependent interpretation of dual-gate performance in nanoscale GaAs MESFETs. The results indicate that the dual-gate configuration provides limited benefit at the baseline geometry but becomes more effective after dimensional scaling, where leakage and electrostatic control become more critical. This prevents an over generalized conclusion and shows that the benefit of the dual-gate structure depends on device scale.

The rest of the paper is organized as follows. In Section 2, the device structures, material assumptions, and numerical methods used in COMSOL Multiphysics are addressed. In Section 3, the results from the simulations for both models are provided. In Section 4, out interpretation of the results is given. In Section 5, conclusions are drawn.

2 Device Structure and Simulation Methodology

2.1 Device Concept

All devices under consideration in this study were depletion mode n-channel GaAs MESFETs. The gate was modeled as a Schottky contact, and source and drain contacts were modeled as ohmic contacts. The geometry for this study is based on an existing published nanoscale MESFET configuration [13]. In the

present work, this reproduced baseline structure is defined as Model 1. It was used as the calibration reference for the numerical setup.

The reference structure in [13] uses a gate length of 10 nm, a device width of 40 nm, a device height of 5 nm, a source width of 10 nm, a drain width of 10 nm, and an n-type doping concentration of $1 \times 10^{20}\,\mathrm{cm}^{-3}$, the same baseline dimensions used for Model 1. Therefore, before introducing the modified structures, Model 1 was implemented in COMSOL Multiphysics to reproduce the behavior of the published reference model. The same numerical setup was then retained for the remaining models so that any observed performance differences could be attributed to gate configuration and scaling rather than to changes in the simulation procedure.

To clarify the investigated device structures, Figure 1 shows the four MESFET configurations used in this work. Model 1 is the baseline single-gate device reproduced from [13]. Model 2 keeps the baseline device dimensions but replaces the single gate with two separated gate segments. Model 3 is the scaled single-gate structure, while Model 4 is the scaled dual-gate structure. The corresponding geometrical dimensions are summarized in Table 1.

This design therefore considers four simulation cases: Model 1 as the baseline single-gate structure, Model 2 as the baseline dual-gate structure, Model 3 as the scaled single-gate structure, and Model 4 as the scaled dual-gate structure.

The scaling procedure in Table 1 was applied consistently to the corresponding single-gate and dual-gate pairs. Model 1 and Model 2 retained the same baseline dimensions, so their comparison isolates the effect of replacing one 10 nm gate with two 5 nm gate segments. Model 3 and Model 4 represent the scaled pair, where the total gate length was reduced from 10 nm to 8 nm, corresponding to a 20% reduction. The device width was reduced from 40 nm to 24 nm, corresponding to a 40% reduction, while the source and drain widths were each reduced from 10 nm to 5 nm, corresponding to a 50% reduction. The device height and n-type doping concentration were kept unchanged. Therefore, the study did not assume that scaling has no effect on the dual-gate device; rather, it evaluated whether the dual-gate configuration can better suppress the leakage increase caused by scaling compared with the corresponding single-gate structure.

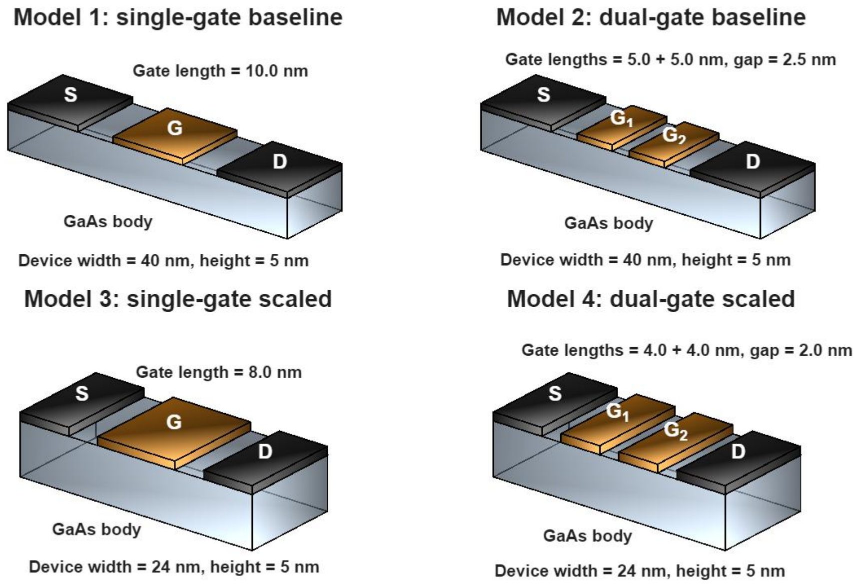


Figure 1 Three-dimensional schematic of the investigated GaAs MESFET structures: Model 1, baseline single-gate device; Model 2, baseline dual-gate device; Model 3, scaled single-gate device; and Model 4, scaled dual-gate device. The schematic clarifies the gate.

Table 1 Geometrical dimensions of the proposed MESFET models.

Description	Main Model	Model 2	Model 3	Model 4
Gate length	10 nm	2 × 5 nm	8 nm	2 × 4 nm
Device width	40 nm	40 nm	24 nm	24 nm
Device height	5 nm	5 nm	5 nm	5 nm
Source width	10 nm	10 nm	5 nm	5 nm
Drain width	10 nm	10 nm	5 nm	5 nm
N-Type doping		1e20[1/cm^3]		

2.2 Material and Physical Assumptions

GaAs was chosen for its well-known high-speed and microwave field-effect device characteristics [16]. The operation of a MESFET relies on the modulation of a depletion region that is created below a Schottky gate. A change in gate voltage causes a change in depletion width, hence affecting the channel of current flow. For a depletion-mode device, a channel exists even when the gate is biased at zero voltage.

The underlying transport model in the COMSOL Semiconductor Module is based on the coupled semiconductor equations, which include Poisson's equation as well as continuity equations for both electrons and holes, together with the drift

diffusion relations. The governing equations can be written in compact form as follows:

$$\nabla \cdot (\varepsilon \nabla \psi) = -q(p - n + N_D^+ - N_A^-) \quad (1)$$
$$\nabla \cdot \mathbf{J}_n = qR, \nabla \cdot \mathbf{J}_p = -qR$$
$$\mathbf{J}_n = q\mu_n n \nabla \phi_n, \mathbf{J}_p = q\mu_p p \nabla \phi_p$$

where ψ is the electrostatic potential, ε the permittivity, n and p the carrier concentrations, N_D^+ and N_A^- the ionized dopants, $\mathbf{J}_n$ and $\mathbf{J}_p$ the current densities, μ_n and μ_p the carrier mobilities, and ϕ_n and ϕ_p the quasi-Fermi potentials. These equations yield the self-consistent electrical solution from which the electron concentration profiles and the drain current may be obtained.

In the current work, emphasis is placed on comparative behavior rather than optimization of a device in absolute terms. As a result, it was decided that identical assumptions regarding the material, contact definitions, and biasing framework would be employed in all four models.

2.3 Numerical implementation in COMSOL

The simulations were carried out using the COMSOL Multiphysics software and its Semiconductor Module. A baseline structure was first reconstructed and solved to ensure that the current-voltage characteristic and charge distribution follow a certain trend similar to that of a reference device. Once this step was completed, three additional models were created by varying the gate configuration and dimensions as described in Section 2.1.

The gate contact was implemented as an ideal Schottky metal contact in COMSOL Multiphysics. The metal work function used for the Schottky gate was set to $\Phi_M = 4.5$ eV. Since the GaAs electron affinity is $\chi = 4.07$ eV, the corresponding ideal Schottky barrier height is $\Phi_B = \Phi_M - \chi = 0.43$ eV. The same Schottky-contact definition was applied to all four models to ensure that the comparison reflects gate configuration and scaling effects rather than changes in the contact boundary condition.

The direct current characteristics were obtained by a stationary study. For a particular device, the drain voltage was varied over a range while the gate voltage was set to a set of values, namely $V_G = 0$ V, 1 V, and 2 V. In addition, electron concentration contours were obtained at $V_D = 0$ V for the same set of gate bias conditions in order to visualize the device behavior.

The mesh was refined in the gate and contact regions to resolve steep gradients in the electric field and carrier concentration. Convergence was verified for all

four models using consistent solver tolerances. The same meshing strategy was applied uniformly across all models.

The present COMSOL implementation was restricted to semiconductor electrostatic and DC transport simulation, while electro-thermal coupling was not included in the current model.

2.4 Evaluation Criteria

Two outputs were used as comparison metrics: the spatial electron concentration, which directly indicates the gate's ability to deplete the channel, and the output characteristic $I_D - V_D$ on both linear and logarithmic scales. The logarithmic scale is of particular importance because any small difference in leakage can be significant if considered over orders of magnitude.

In this study, near-off-state behavior refers to the low-current operating condition obtained at the highest applied gate bias, $V_G = 2$ V, under high drain bias $V_D =$ 9 V. This condition is used to evaluate unwanted drain-to-source leakage because the channel is strongly depleted and the leakage component becomes more visible, particularly in the logarithmic $I_D - V_D$ response. From the perspective of the scaled device, this condition is important because it indicates the strength of electrostatic confinement and the ability of the gate structure to suppress parasitic current.

3 Results

3.1 Baseline Structures: Main Model and Model 2

The first such comparison was carried out between the base single-gate device and the dual-gate device with the same overall dimensions. The purpose behind this particular model was to compare how much improvement is achieved by changing one gate to two gates while keeping the size of the device constant.

The electron concentration contours for the Main Model at $V_D = 0$ V for $V_G =$ 0 V, 1 V, and 2 V are given in Figure 1, and output characteristics for these values in Figure 2. The electron concentration contours for Model 2 in Figures 3 and 4.

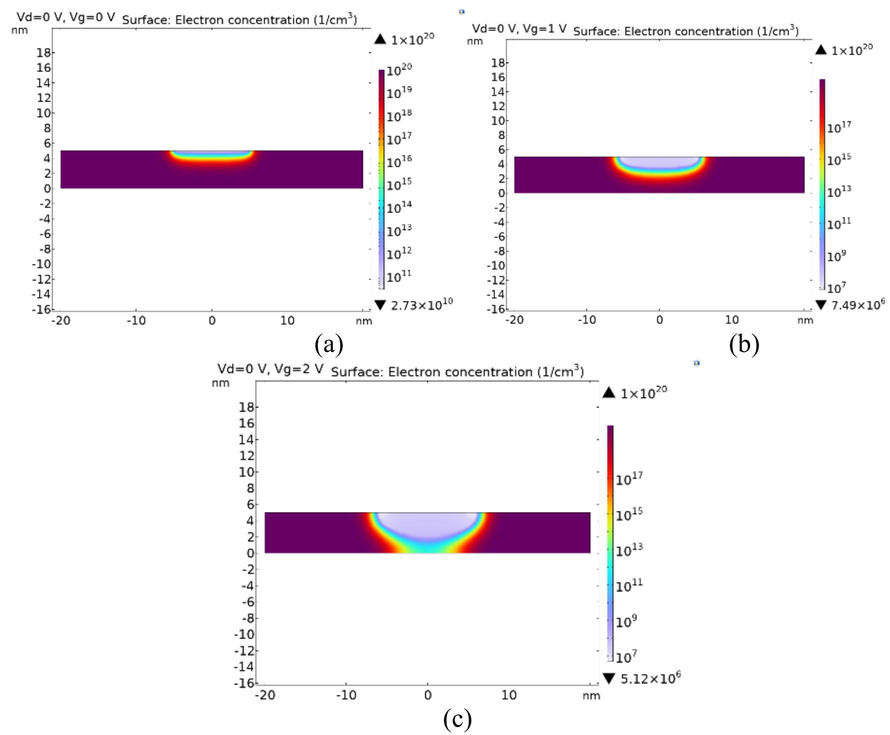


Figure 2 Electron concentration contours of the main model at $V_D = 0$ V for (a) $V_G = 0$ V, (b) $V_G = 1$ V, and (c) $V_G = 2$ V.

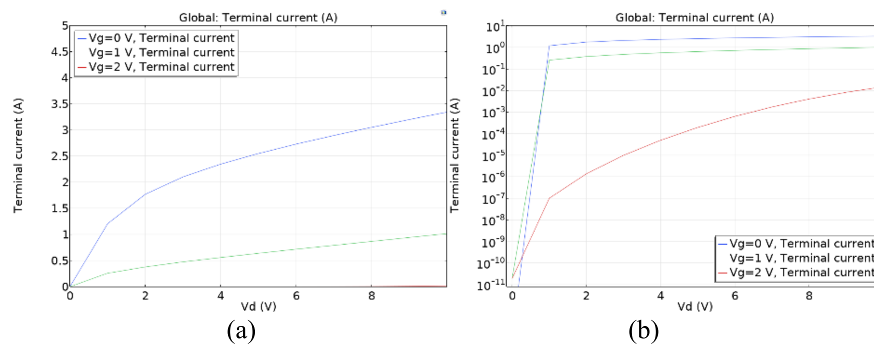
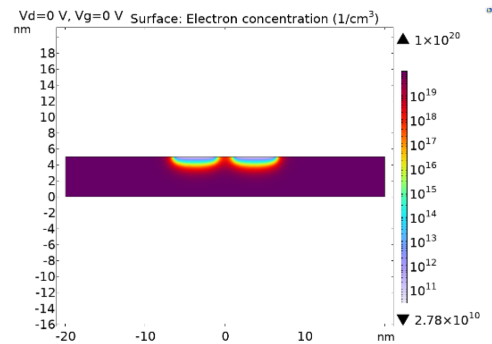
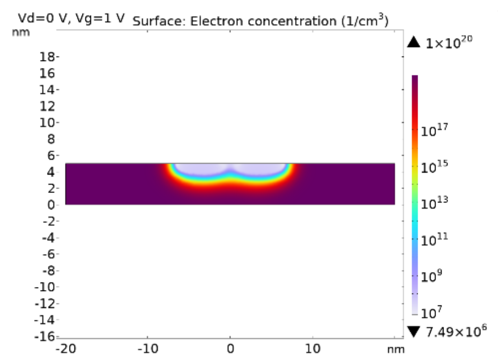


Figure 3 Output characteristics of the main model, shown in (a) linear scale and (b) logarithmic scale.



(a)



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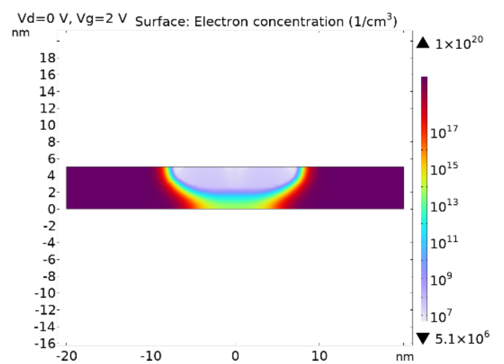
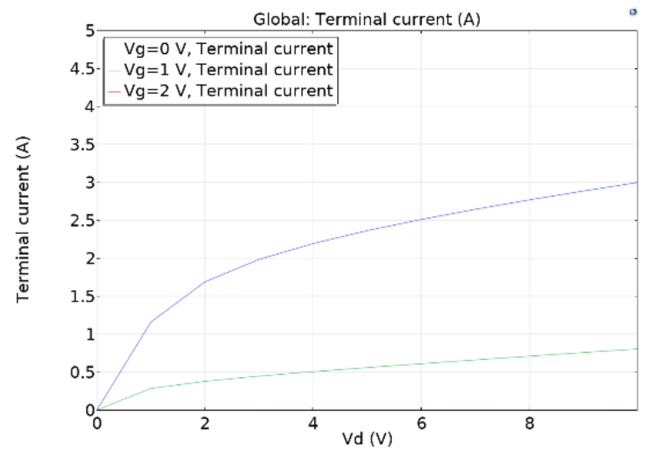
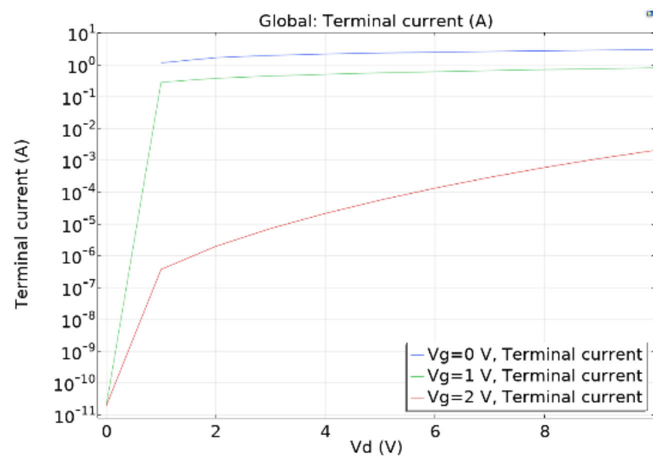


(c)

Figure 4 Electron concentration contours of Model 2 at $V_D = 0$ V for (a) $V_G = 0$ V, (b) $V_G = 1$ V, and (c) $V_G = 2$ V.



(a)



(b)

Figure 5 Output characteristics of Model 2, shown in (a) linear scale and (b) logarithmic scale.

At the baseline geometry, both devices showed similar current-voltage behavior. Gate control of the channel is observed in both structures and the output curves do not show a large separation. This indicates that the dual-gate configuration does not automatically provide a substantial advantage when the baseline device dimensions are retained.

The logarithmic $I_D - V_D$ response provides a clearer view of the low-current region. At the baseline scale, the improvement from the dual-gate structure is limited, although the extracted leakage values show better near-off control for Model 2. Therefore, the baseline comparison does not support a broad claim of universal dual-gate superiority; rather, it indicates that the benefit depends on device scale and operating condition.

The interpretation here is that, if we use the original dimensions, the channel remains adequately controlled by the single Schottky gate and the additional gate provides no measurable electrostatic benefit at this geometry. In other words, the device is not yet scaled down enough for the multi-gate structure to provide its main advantage.

3.2 Reduced Structures: Model 3 and Model 4

The second comparison is related to the more critical part of this work. After reducing the dimensions of the device, the problem of electrostatics will worsen and the role of gate structure should become more pronounced.

Figures 5 and 6 show the electron concentration and output characteristics of the reduced single gate device, Model 3. Figures 7 and 8 show the electron concentration and output characteristics of the reduced dual gate device, Model 4.

In the scaled devices, the difference between the two gate configurations becomes clearer. Both models show leakage at high drain bias, which is expected because the reduced geometry increases the electrostatic demand on the gate. However, the scaled single-gate MESFET shows a higher leakage level than the scaled dual-gate structure. This indicates that the dual-gate configuration provides stronger channel confinement and better suppression of unwanted drain-to-source current.

This contrast can be observed more clearly under the near-off-state condition, where $V_G = 2$ V and the suppression of unwanted drain-to-source current is more critical. When the drain voltage is high, the reduced single gate device (Model 3) allows more parasitic current to flow, whereas the reduced dual gate structure (Model 4) suppresses the leakage to a significantly low level (Figure 9). The electron concentration plot also supports these results, indicating more control in the channel region in the dual gate structure.

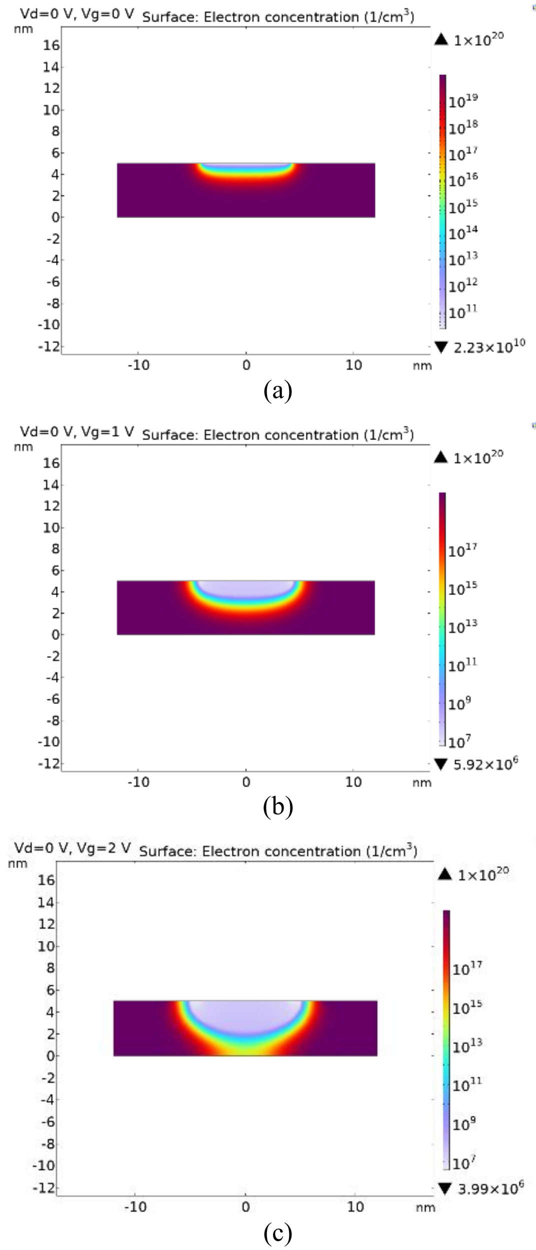
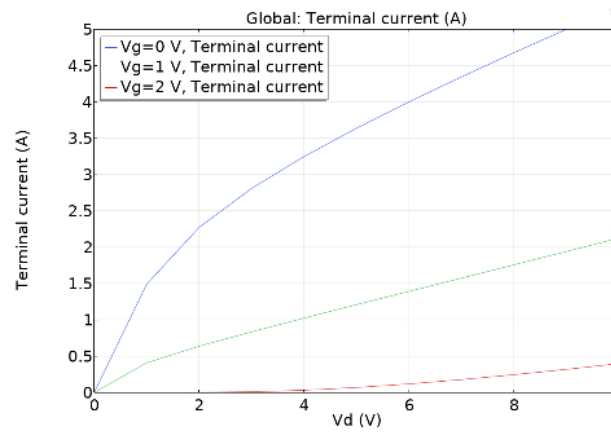
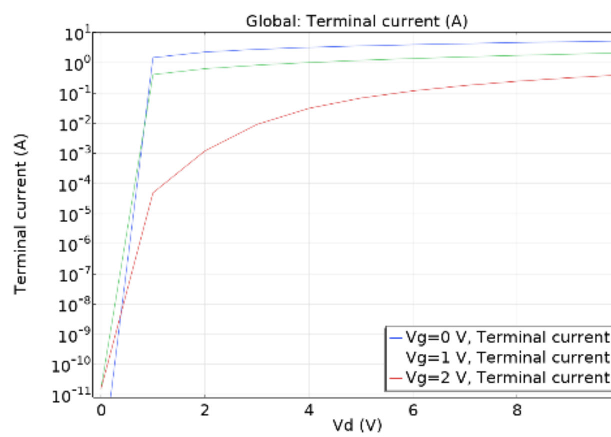


Figure 6 Electron concentration contours of Model 3 at $V_D = 0$ V for (a) $V_G = 0$ V, (b) $V_G = 1$ V, and (c) $V_G = 2$ V.



(a)



(b)

Figure 7 Output characteristics of Model 3, shown in (a) linear scale and (b) logarithmic scale.

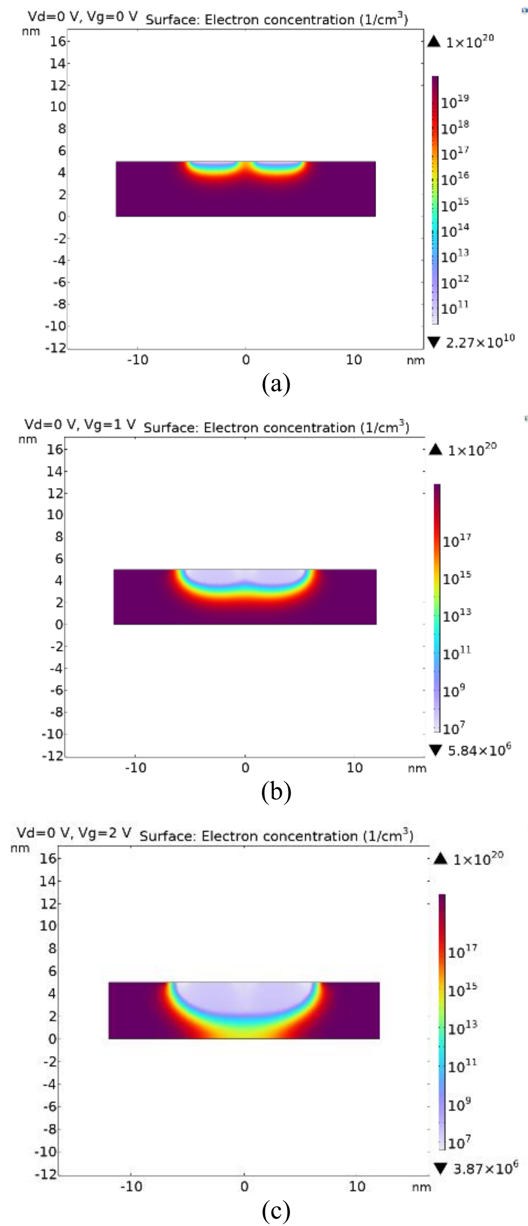
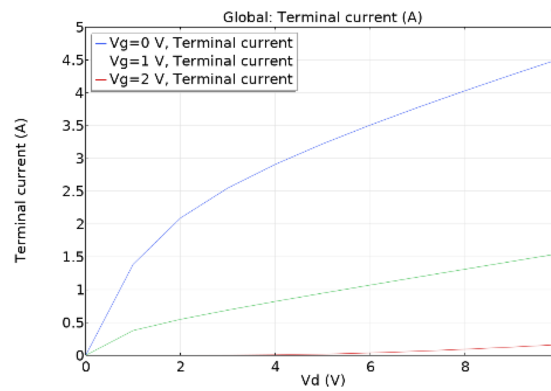
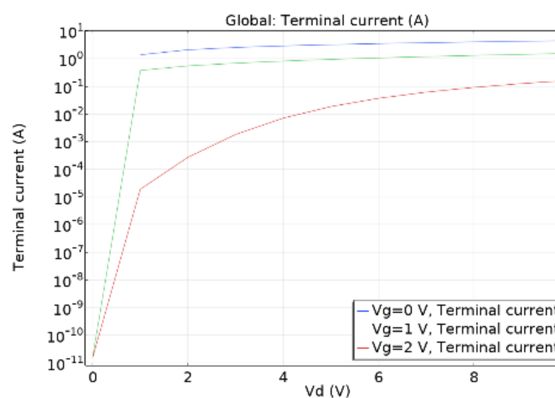


Figure 8 Electron concentration contours of Model 4 at $V_D = 0$ V for (a) $V_G = 0$ V, (b) $V_G = 1$ V, and (c) $V_G = 2$ V.



(a)



(b)

Figure 9 Output characteristics of Model 4, shown in (a) linear scale and (b) logarithmic scale.

The extracted leakage-current comparison for all four MESFET models is summarized in Table 2. The values were extracted at $V_G = 2$ V and $V_D = 9$ V, where the device operates closer to the low-current or near-off regime and the effect of gate control becomes more visible in the logarithmic output response. This comparison is included to quantify the scale-dependent effect of the dual-gate structure, rather than relying only on the visual difference between the output curves.

Table 2 Extracted leakage-current comparison for the baseline and scaled MESFET models.

Bias condition	Model	Gate configuration	Device scale	Extracted leakage current
$V_G = 2$ V, $V_D = 9$ V	Model 1 [13]	Single gate	Baseline	≈ 8 mA
$V_G = 2$ V, $V_D = 9$ V	Model 2	Dual gate	Baseline	≈ 1 mA
$V_G = 2$ V, $V_D = 9$ V	Model 3	Single gate	Scaled	≈ 318 mA
$V_G = 2$ V, $V_D = 9$ V	Model 4	Dual gate	Scaled	≈ 126 mA

Table 2 shows that the dual-gate configuration reduced the extracted leakage current in both the baseline and scaled devices. In the baseline case, the leakage current decreased from approximately 8 mA in Model 1 to approximately 1 mA in Model 2, indicating that the second gate improves electrostatic control even before scaling. However, the absolute difference becomes more important after scaling, where the leakage current decreased from approximately 318 mA in Model 3 to approximately 126 mA in Model 4. This confirms that the dual-gate structure is most relevant under scaled conditions, where leakage becomes more severe and stronger gate control is required.

To provide a more quantitative comparison beyond the contour and output-characteristic plots, additional current-based parameters were extracted from the simulated transfer response at $V_D = 9$ V. The on-current, I_{on}, was taken at $V_G = 0$ V, while the off-current, I_{off}, was taken at $V_G = 2$ V. The switching ratio was then calculated as $I_{\text{on}}/I_{\text{off}}$. These extracted values are summarized in Table 3.

Table 3 Extracted current-based performance parameters of the four MESFET models.

Model	I_{on}	I_{off}	$I_{\text{on}}/I_{\text{off}}$
Model 1 [13]	3.198 A	8.26 mA	387.23
Model 2	2.885 A	1.143 mA	2523.3
Model 3	4.998 A	318.13 mA	15.71
Model 4	4.275 A	126.03 mA	33.92

As Table 3 shows, the performance of dual-gate structure in improving switching performance was verified in two different size devices. For the benchmark devices, Model 2 resulted in an improvement of switching ratio when compared to Model 1 due to a higher reduction of off-current, whereas on-current did not vary much in magnitude. Similarly, for the scaled devices, Model 4 led to an improvement of the switching ratio as compared to Model 3, mainly due to a significant decrease of near-off current from 318.13 mA to 126.03 mA. The switching ratio of scaled dual-gate structure was still lower as compared to

benchmark devices, because scaling increases the leakage, but Model 4 showed better electrostatic suppression capability than Model 3.

4 Discussion

The findings lead to a design choice based on scale rather than an absolute conclusion that any specific gate configuration is universally better. At the base geometry, there is little difference between the two types of gates, except for the fact that both leakage and switching ratios suggest that the dual-gate configuration offers better off-state leakage control. However, at the scaled geometry, the issue became more significant, with the scaled single-gate configuration offering higher leakage and the scaled dual-gate configuration offering stronger electrostatic control.

This type of behavior is also in line with the physical functionality of gate control in scaled devices. For the basic transistor, the channel can be controlled effectively enough using one Schottky gate, such that the second gate does not help much in enhancing the response. After scaling, the reduced device dimensions amplify drain-field penetration and increase leakage significantly. In such a situation, the addition of the second gate gives one more electrostatic constraint on the channel, which accounts for the better leakage performance of Model 4 relative to Model 3.

The logarithmic output response was also important for interpreting the scaled devices. Linear plots mainly emphasize the high-current region, whereas logarithmic plots reveal differences in the near-off-state condition. Therefore, the logarithmic $I_D - V_D$ response was used to evaluate leakage behavior that may be less visible in the linear-scale plots.

Overall, the leakage-current and switching-ratio results support the interpretation that the dual-gate structure is most useful when scaling increases the severity of electrostatic leakage.

5 Conclusion

Comparative COMSOL-based simulations were performed to evaluate four GaAs MESFET structures at both baseline and scaled dimensions. The first model was based on the existing structure with single gates, while models two through four were added to enable comparison with regard to dual gate geometry and scaling within the same computational framework. It was found that the application of a dual gate configuration enabled improved near off-currents control in both cases; however, the latter became significant only after scaling.

The principal finding is that the performance advantage of the dual-gate configuration is scale-dependent. The dual-gate MESFET is not universally superior; its benefit becomes significant only when scaling intensifies electrostatic leakage. This is especially because the dual gate MESFET is relatively more useful as a result of increased scale effects making electrostatic confinement harder. This was evidenced through leakage current and switching ratio performance comparisons.

The present study is limited to DC electrostatic simulation. Future work should address RF small-signal performance, experimental verification, and the impact of process variations on GaAs MESFET devices..

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