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Initial SOC Error Recovery with a CC-RLS-PI Hybrid Estimator

Pemulihan Galat SOC Awal dengan Estimator Hibrida CC-RLS-PI

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Abstract

Coulomb counting (CC) is open-loop and cannot correct a wrong initial State of Charge (SOC). A scheme that adds recursive least squares (RLS) parameter identification and a proportional-integral (PI) correction to CC was proposed for a 260 mAh cell. This study examines that scheme with Thevenin parameters identified offline and held fixed, using Panasonic 18650PF data under static 1C, HWFET and UDDS profiles, initial errors of −2, −20 and −35 percentage points of SOC, and a comparison with CC and with open-circuit-voltage (OCV) initialization. The hybrid estimator first entered the ±2% error band within 1–389 s but never stayed in it. Its mean absolute error (MAE) was 1.5–4.0%, rising to 5.0–7.7% below 40% SOC on the static and HWFET profiles, and it beat CC only when the initial error was at least 2–4 points. In starts at mid-SOC under load without rest, it had a lower MAE than OCV initialization in 7 of 9 cases. The identified polarization resistance changed more than threefold with the forgetting factor. The scheme suits recovery from large initial errors when OCV initialization is unreliable, within an accuracy limit of about 2–4%.

Keywords: State of Charge, Coulomb Counting, initial error, Battery Management System.

Abstrak

*Penghitungan muatan (*Coulomb counting*, CC) bersifat* open-loop *sehingga tidak dapat mengoreksi nilai awal* State of Charge *(SOC) yang keliru. Skema yang menambahkan identifikasi parameter* Recursive Least Square *(RLS) dan koreksi* Proportional-Integral *(PI) pada CC pernah diusulkan untuk sel 260 mAh. Penelitian ini menguji skema tersebut dengan parameter Thevenin yang diidentifikasi secara offline dan dibuat tetap, memakai data sel Panasonic 18650PF pada profil statis 1C, HWFET, dan UDDS, galat awal −2, −20, dan −35 poin persentase SOC, serta perbandingan dengan CC dan inisialisasi tegangan rangkaian terbuka (OCV). Estimator hibrida pertama kali masuk ke pita ±2% dalam 1–389 s tetapi tidak pernah bertahan di dalamnya. Galat absolut rata-rata (MAE) sebesar 1,5–4,0%, naik menjadi 5,0–7,7% di bawah SOC 40% pada profil statis dan HWFET, dan baru lebih rendah daripada CC bila galat awal minimal 2–4 poin. Pada start di SOC menengah tanpa istirahat, MAE-nya lebih rendah daripada inisialisasi OCV pada 7 dari 9 kasus. Resistansi polarisasi hasil identifikasi berubah lebih dari tiga kali lipat terhadap faktor pelupa. Skema ini cocok untuk memulihkan galat awal besar saat inisialisasi OCV tidak andal, dengan batas akurasi sekitar 2–4%.*

Kata Kunci: State of Charge, Coulomb Counting, *galat awal, Sistem Manajemen Baterai.*

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1 Introduction

The growing adoption of electric vehicles (EVs) has intensified research on reliable battery monitoring [1]. The state of charge (SOC) is a key quantity of the Battery Management System (BMS) of lithium-ion batteries, and its accuracy affects range prediction, safety and battery life [2],[3]. Many estimation techniques have been reviewed, broadly grouped into model-based and data-driven methods [4]–[6], each with trade-offs in accuracy, complexity and computational cost.

Coulomb counting (CC) estimates SOC by integrating the measured current [7]–[9]. It is simple and cheap, but it is open-loop: nothing in the algorithm can reduce an error that is already present [8],[9]. Two error sources should be kept apart. The first is the initialization error, because the true SOC at start-up is rarely known: a battery pack is seldom powered on fully charged and rested. The second is the integrated measurement error, because the integrator accumulates sensor bias and noise, so that a small bias grows with time. The first gives a constant offset and the second a growing drift. Section 2.2 formalizes this split, and the present study evaluates the first component.

Several studies refine CC or combine it with other methods. Ng et al. corrected the integration for charging and operating efficiency [10]; Zhao et al. combined CC with least-squares estimation [7]; Mohammadi added an uncertainty evaluation to an improved CC algorithm [11]; Kumar et al. combined CC with fuzzy logic [12]; and Fahmy et al. paired CC with an adaptive unscented Kalman filter whose model parameters were found by an optimizer [13]. Most of these act on the integration itself or add a filter, and, to our knowledge, they do not report recovery from a deliberately wrong initial SOC on standard drive cycles. Model-based filters such as the extended Kalman filter (EKF) [14] and its adaptive variants [15] close the loop through the voltage measurement and can in principle forget a wrong initial state, but they need a calibrated model and filter tuning, and their computational load is a concern on low-cost BMS hardware [16],[17].

In practice, the initial SOC is often read from the open-circuit voltage (OCV) after a rest period [8],[18],[19]. When no rest is available, for example at a key-on soon after driving, the terminal voltage still contains the ohmic and polarization drops, and the OCV-based initial value inherits that offset. Kustiman et al. [19] proposed adding RLS parameter identification and a proportional-integral (PI) controller to CC to correct a false initial SOC. On a 260 mAh cell under a pulsed 260 mA load, they reported a mean absolute error (MAE) of 0.41–0.59% for initial SOCs of 98%, 80% and 65%, with convergence in about 200 s. It remains unclear how this scheme behaves under standard dynamic drive cycles, how fast and how stably it recovers, how it compares with the simpler OCV initialization, and how sensitive it is to the PI gains and the identified parameters.

This paper therefore evaluates the CC-RLS-PI scheme of [19], with Thevenin parameters identified offline and held fixed, on the Panasonic 18650PF cell under static 1C, HWFET and UDDS profiles. The contributions are: (i) an evaluation with transient metrics (first entry into an error band, time spent in the band, and error by SOC range) rather than a single convergence time; (ii) the conditions under which the correction helps, given by the break-even initial error and a comparison with OCV initialization, including starts at mid-SOC without rest; (iii) the sensitivity of the outcome to the PI gains and to the RLS forgetting factor, which governs the identified polarization resistance; and (iv) a quantitative comparison with [19]. We do not propose a new estimator, and we make no claim about efficiency relative to EKF.

2 Method

2.1 Data and Reference Capacity

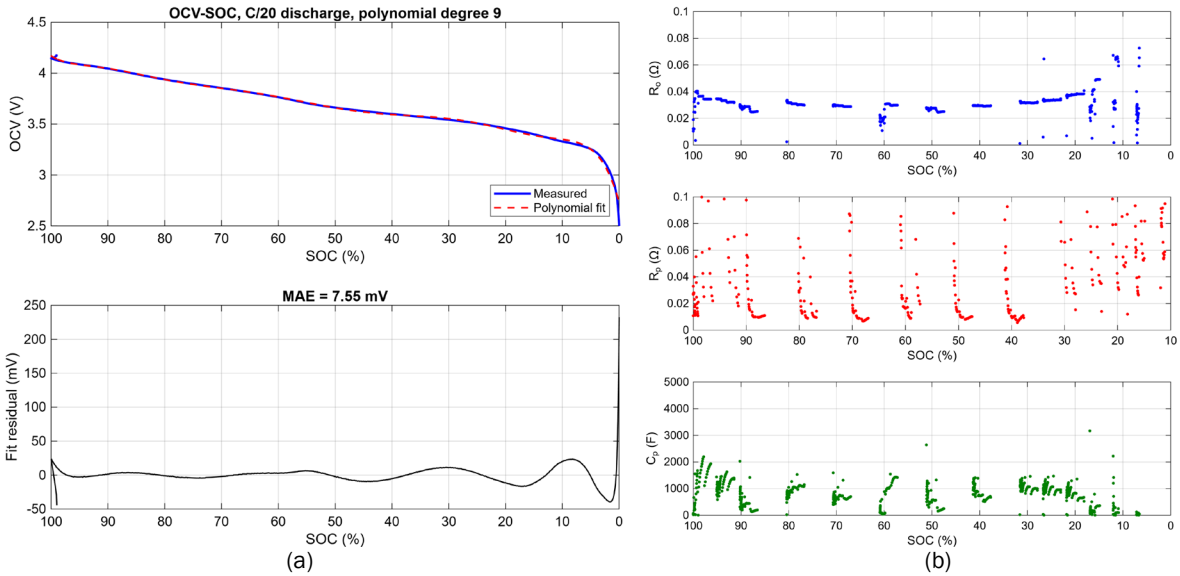


Figure 1. (a) OCV–SOC curve of the C/20 test with its 9th-degree polynomial fit (top) and the fit residual (bottom); (b) R_0, R_p and C_p identified at each HPPC sample versus SOC.

Secondary discharge data of a Panasonic 18650PF cell [20] (nominal 2.9 Ah, 3.6 V) recorded in a thermal chamber at 25 °C were used. The C/20 discharge test gave the usable capacity C_n = 2.9677 Ah and the OCV–SOC relation, which was fitted with a 9th-degree polynomial $f(\cdot)$ [18],[21],[22]. The mean absolute fit error is 7.55 mV, and 6.90 mV and 7.39 mV on the training and test parts of a 70:30 split (Figure 1a). Degrees 11 and 13 lowered the test error to 5.4 and 3.4 mV, but degree 9 was kept from the original analysis. The polynomial is monotonic with a minimum slope of 0.315 V per unit SOC near 37% SOC, where an OCV error of 10 mV corresponds to an SOC error of 3.2 points.

The reference SOC of each test profile was obtained by integrating its own measured current from a fully charged initial state with C_n. The cell was charged by CC-CV (4.2 V, 50 mA cut-off) before each test, so the true initial SOC is 100%; the C/20 test supplies only C_n and the OCV curve. Three current profiles were used (Figure 2): a constant 2.9 A (1C) discharge, the HWFET highway cycle with continuous current fluctuation (peak 5.4 A), and the UDDS urban cycle with stop-and-go phases and near-zero current intervals (peak 7.3 A); both drive cycles include regenerative phases. They have 3485, 7308 and 22 125 samples at 1 s. The equivalent circuit parameters were identified from the 5-pulse HPPC test at 25 °C. All computations were run in MATLAB R2026b, and the script that regenerates every table and figure is provided as supplementary material.

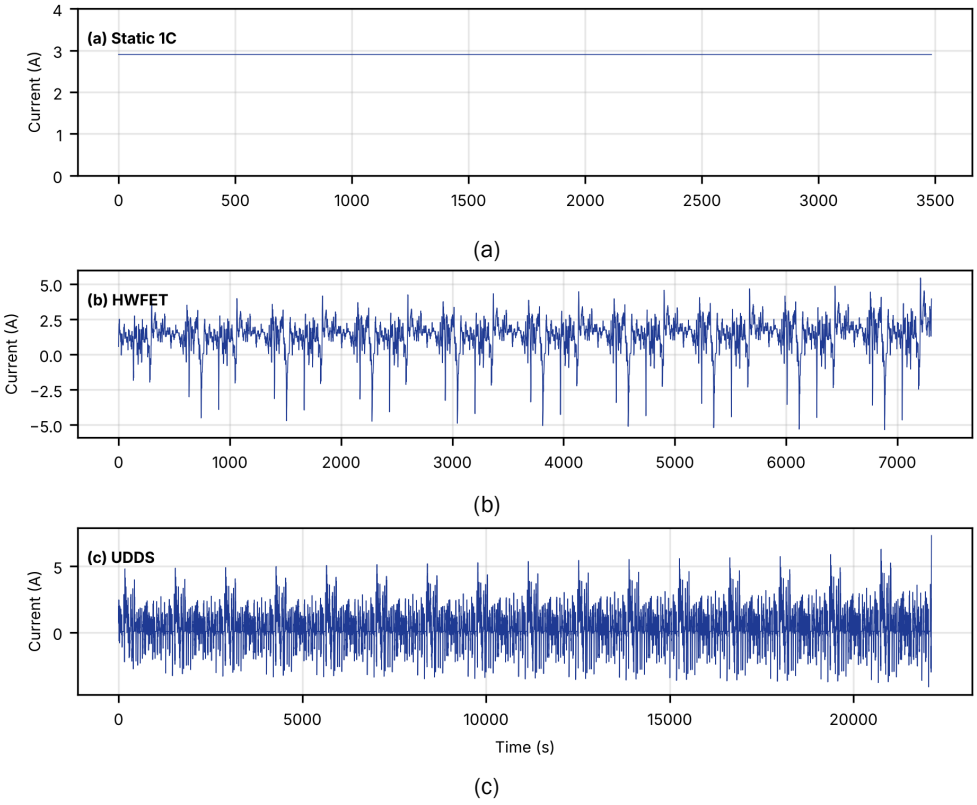


Figure 2. Discharge current profiles used for testing: (a) static 1C, (b) HWFET, (c) UDDS (positive current is discharge).

2.2 Conventional Coulomb Counting and Its Error

The conventional CC estimate is given by (1), where $SOC_0(t_0)$ is the initial SOC, η is the coulombic efficiency, C_n is the usable capacity and $I(t)$ is the discharge current. This estimate is the baseline against which the hybrid estimator is compared throughout the paper.

$$SOC(t) = SOC_0(t_0) - \frac{\eta}{C_n}\int_{t_0}^{t} I\,(t)\,dt \tag{1}$$

Let the measured current be $I_{meas} = I_{true} + e_I$, where e_I contains sensor bias and noise. Subtracting the true SOC from (1) gives the CC error (2), with the initialization error (3).

$$e_{CC}(t) = \widehat{SOC}_{CC}(t) - SOC_{true}(t) = e_{init} - \frac{\eta}{C_n}\int_{t_0}^{t} e_I\,(\tau)\,d\tau \tag{2}$$

$$e_{init} = \widehat{SOC}_0(t_0) - SOC_{true}(t_0) \tag{3}$$

The first term of (2) is a constant offset and the second is a drift. The data used here carry laboratory-grade current measurement, so the drift term is numerically negligible and $e_{CC} \approx e_{init}$. Moreover, because the reference SOC is itself the CC integral of the same current, CC with a correct initial value coincides with the reference by construction; this is a property of the reference and not a result about CC (see Limitations).

2.3 Equivalent Circuit Model

The cell was represented by a first-order Thevenin model (1RC, Figure 3): an ohmic resistance R_0 in series with a parallel branch R_p–C_p for polarization, a widely used structure for online SOC and parameter estimation in EVs [23]. Following [19], the discrete-time terminal voltage obtained with the bilinear transform is (4), where V_t is the terminal voltage, V_{oc} is the open-circuit voltage, I is the discharge current (positive in discharge) and a_1, b_0, b_1 follow from (5)–(7) with the sampling period T. The sign of a_1 is chosen here so that (8)–(10), which recover the physical parameters, are consistent with (4)–(7).

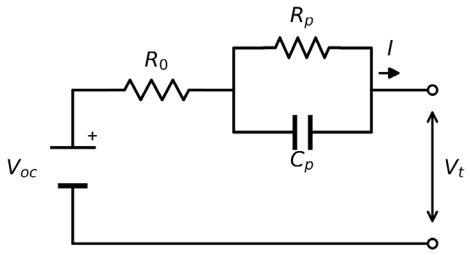


Figure 3. First-order Thevenin equivalent circuit (1RC), topology after [19].

$$V_t(k) = V_{oc}(k) + a_1[V_t(k-1) - V_{oc}(k-1)] - b_0 I(k) - b_1 I(k-1) \tag{4}$$

$$a_1 = \frac{2R_pC_p - T}{2R_pC_p + T} \tag{5}$$

$$b_0 = \frac{R_0T + R_pT + 2R_0R_pC_p}{T + 2R_pC_p} \tag{6}$$

$$b_1 = \frac{R_0T + R_pT - 2R_0R_pC_p}{T + 2R_pC_p} \tag{7}$$

$$R_0 = \frac{b_0 - b_1}{1 + a_1} \tag{8}$$

$$R_p = \frac{2(a_1b_0 + b_1)}{1 - a_1^2} \tag{9}$$

$$C_p = \frac{T(1 + a_1)^2}{4(a_1b_0 + b_1)} \tag{10}$$

2.4 Offline RLS Identification

The coefficients $\theta = [a_1\ b_0\ b_1]^T$ were estimated by RLS, a common choice for equivalent-circuit parameter identification [24],[25], using (11)–(13), where K_k is the gain, P_k the covariance matrix, λ the forgetting factor, $y(k) = V_t(k) - f(SOC_{ref}(k))$ the output and $\varphi_k = [y(k\text{-}1), -I(k), -I(k\text{-}1)]^T$ the regressor. SOC_{ref} is the CC value from the known initial state of the HPPC test.

$$\hat{\theta}_k = \hat{\theta}_{k-1} + K_k\left(y(k) - \varphi_k^T\hat{\theta}_{k-1}\right) \tag{11}$$

$$K_k = \frac{P_{k-1}\varphi_k}{\lambda + \varphi_k^T P_{k-1}\varphi_k} \tag{12}$$

$$P_k = \frac{1}{\lambda}(P_{k-1} - K_k\varphi_k^T P_{k-1}) \tag{13}$$

The settings were $\lambda = 0.985$, $P(0) = 1000\ I_3$, $\theta(0) = 0$ and $T = 1$ s. Each estimate of θ was converted to R_0, R_p and C_p by (8)–(10), and the medians over the samples with SOC between 20% and 80% and $|I| > 3$ A (233 samples) were retained: $R_0 = 0.0301\ \Omega$, $R_p = 0.0242\ \Omega$, $C_p = 887$ F and $\tau = R_pC_p = 21.5$ s. The identification is

therefore run once, offline, and the parameters are held fixed in the estimator; no RLS runs during estimation. Figure 1b shows that R_0 is stable near 0.03 Ω at mid-SOC, whereas R_p and C_p scatter widely (R_p from about 0.01 to 0.1 Ω), so R_p is poorly determined by the data.

2.5 CC-RLS-PI Hybrid Estimator

Following [19], CC supplies $SOC_{CC}(k) = SOC_{CC}(k-1) - (\eta T_s/3600C_n)I(k)$, the RLS-identified model reconstructs the OCV from the measured voltage and current, and a PI controller, in the spirit of a proportional-integral observer [26], drives the difference between the reconstructed OCV and the OCV predicted from the corrected SOC to zero (Figure 4). Assuming $V_{oc}(k) \approx V_{oc}(k-1)$ in (4), the reconstructed OCV is (14).

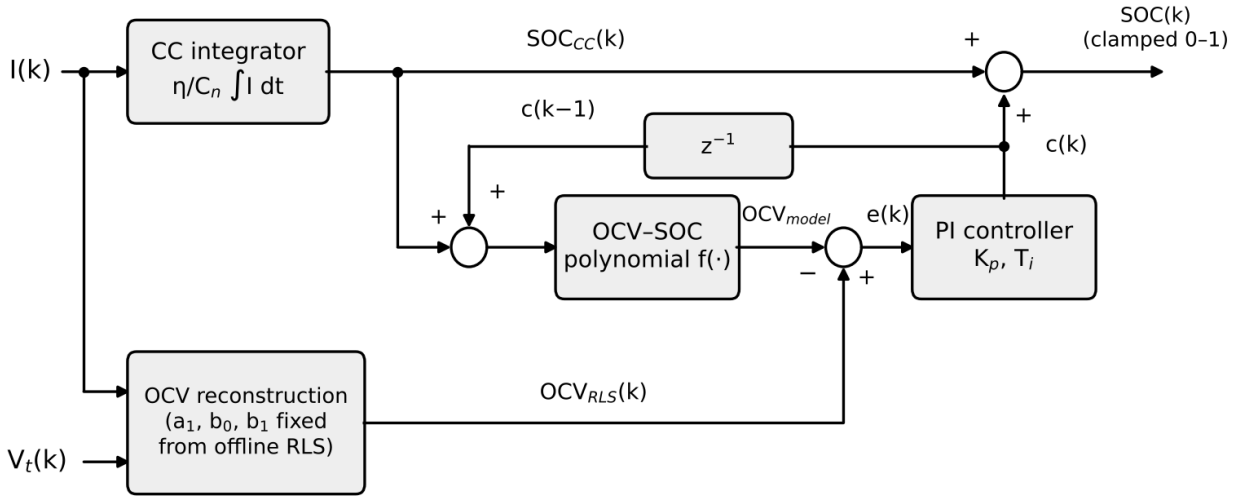


Figure 4. Block diagram of the CC-RLS-PI hybrid estimator. The coefficients a_1, b_0, b_1 come from the offline RLS identification and are fixed.

$$OCV_{RLS}(k) = \frac{V_t(k) - a_1 V_t(k-1) + b_0 I(k) + b_1 I(k-1)}{1 - a_1} \tag{14}$$

The OCV residual is (15), where $f(\cdot)$ is the polynomial of Section 2.1 and $[\cdot]_0^1$ clips to [0, 1]. The velocity-form digital PI law is (16), with K_p in SOC per volt, T_s the sampling time and T_i the integral time, so that the integral gain is $K_i = K_p T_s/T_i$. The estimate is (17).

$$e(k) = OCV_{RLS}(k) - f([SOC_{CC}(k) + c(k-1)]_0^1) \tag{15}$$

$$c(k) = c(k-1) + K_p\left(1 + \frac{T_s}{T_i}\right)e(k) - K_p e(k-1) \tag{16}$$

$$SOC(k) = [SOC_{CC}(k) + c(k)]_0^1 \tag{17}$$

When the clip is active, $c(k)$ is set to the value that reproduces the clipped SOC, which serves as the anti-windup; the CC integrator is never reset. Since $1 - a_1 = 2T/(T + 2\tau) \approx 0.045$ here, errors in V_t are amplified about 22 times in (14). The residual $e(k)$ therefore carries spikes of up to several volts under dynamic loads (Figure 7), and the gains must be small.

The gains K_p (SOC per volt) and T_i (s) were set per profile (Table 1). They come from the original heuristic tuning and were afterwards checked on a grid of $K_p \in \{0.001, 0.002, 0.005, 0.01, 0.02, 0.05\}$ and $T_i \in \{0.03, 0.1, 0.5, 1, 2, 5\}$ s (36 pairs per profile). A pair was called feasible when the worst-case maximum error after first entry into the ±2% band (over Scenarios A–C) is at most 13% and the MAE of Scenario C is within 1.25 times the best MAE on that profile. A faster first entry is traded against a noisier correction, measured by the standard deviation of the per-second change of $c(k)$ after first entry. A value $T_i < T_s$ is admissible in the velocity form (16), where the effective gain on $e(k)$ is $K_p(1 + T_s/T_i)$.

2.6 Test Scenarios and Metrics

Three initialization scenarios assumed an initial SOC of 98% (A), 80% (B) and 65% (C) against a true value of 100%, that is, e_{init} = −2, −20 and −35 percentage points of SOC (the absolute difference of SOC in %, not a relative error), for both estimators on all three profiles (18 runs). Errors, MAE and RMSE are expressed in the same unit, and "points" below always means percentage points of SOC. Three further tests used the same estimators. Positive errors: starts at a true SOC of 60% with assumed values 2, 20 and 35 points higher. Mid-profile starts: runs begin where the true SOC first falls to 80%, 60% and 40% while the cell is under load and without a preceding rest, to emulate a key-on during use; here the hybrid estimator is given an initial error of +20 points. OCV initialization: CC started from the SOC obtained by inverting $f(\cdot)$ at (a) the rest voltage before the test, (b) the first loaded voltage $V_t(1)$, and (c) $V_t(1) + I(1)R_0$, without any further correction.

Accuracy is reported by the MAE (18) and the RMSE (19), where N is the number of samples. Recovery is described by the first entry time t_1, the earliest time at which the absolute SOC error is at most 2 points; the share of samples inside the ±2% band before the true SOC falls below 30% ("in band"); the settling time, the earliest time after which the error stays inside a band until SOC < 30% (∞ if it never does; t_{10} for the ±10% band); the maximum absolute error after t_1; and the MAE by SOC range. The break-even initial error is the smallest tested value of $|e_{init}|$ (1, 2, 3, 4, 5, 7, 10, 15, 20 and 35 points) at which the hybrid MAE is below the CC MAE. No metric is averaged across scenarios, because the CC error in these tests equals the imposed offset and any average would only reflect that choice. The computational load is reported by operation counts and not by run time (Section 3.7).

$$MAE = \frac{100\%}{N}\sum_{k=1}^{N}|SOC_{est}(k) - SOC_{actual}(k)| \tag{18}$$

$$RMSE = 100\% \times \sqrt{\frac{1}{N}\sum_{k=1}^{N}\left(SOC_{est}(k) - SOC_{actual}(k)\right)^2} \tag{19}$$

Table 1. Simulation settings.

Item	Value	Item	Value
Cell, temperature	Panasonic 18650PF, 25 °C	Gains static 1C	K_p = 0.002, T_i = 0.03 s
Capacity C_n	2.9677 Ah	Gains HWFET	K_p = 0.02, T_i = 2 s
Coulombic efficiency η	1	Gains UDDS	K_p = 0.01, T_i = 2 s
Sampling period T_s	1 s	Assumed initial SOC (true 100%)	A: 98%, B: 80%, C: 65%
OCV–SOC fit	degree 9, MAE 7.55 mV	Error bands	±2 and ±10 points
RLS settings	λ = 0.985, $P(0)$ = 1000 I_3, $\theta(0)$ = 0	Low-SOC region	SOC < 30%
R_0, R_p, C_p (fixed)	0.0301 Ω, 0.0242 Ω, 887 F	Identification data	HPPC, 5 pulses, offline
Time constant τ	21.5 s	Software	MATLAB R2026b

3 Results and Discussion

3.1 Conventional CC: Offset Retention

Table 2 gives the MAE of both estimators for the nine combinations of profile and scenario. For CC, the MAE reproduces the imposed offset within 0.005 points (2.000, 20.000 and 35.000 on the static profile, and at most 0.004 away on HWFET and UDDS), and the CC trajectories run parallel to the reference (Figure 5). This is the retention of an initial condition by an open-loop integrator. With a noise-free current it is fixed by the choice of the scenario and not by a property of the algorithm, so no aggregate MAE is reported.

Table 2. MAE (% of SOC) of CC and the hybrid CC-RLS-PI for initial errors in percentage points of SOC (A, B, C).

Load profile	Method	A (−2)	B (−20)	C (−35)
Static 1C	CC	2.000	20.000	35.000
	CC-RLS-PI	3.864	3.920	3.981
HWFET	CC	2.004	20.004	35.004
	CC-RLS-PI	2.924	3.117	3.309
UDDS	CC	1.999	19.999	34.999
	CC-RLS-PI	1.513	1.634	1.760

3.2 Recovery of the Hybrid Estimator

The hybrid MAE (Table 2) is 1.5–4.0% and almost independent of the initial error: from Scenario A to C it changes from 3.864 to 3.981 on the static profile, from 2.924 to 3.309 on HWFET and from 1.513 to 1.760 on UDDS, while the imposed offset grows about 17-fold. The estimate leaves the initial offset quickly (Figure 5), first entering the ±2% band after 1, 24 and 30 s on the static profile (Scenarios A, B, C), 9, 175 and 244 s on HWFET and 5, 344 and 389 s on UDDS (Table 3). The entry time grows with the initial error and, for the dynamic profiles, with the smaller integral gain $K_i = K_p T_s / T_i$ (0.0667, 0.0100 and 0.0050 for the static, HWFET and UDDS gains). Figure 7 shows the mechanism: $c(k)$ rises to the offset (about 35 points in Scenario C) within the first minutes, while $e(k)$ contains spikes caused by the voltage amplification of (14).

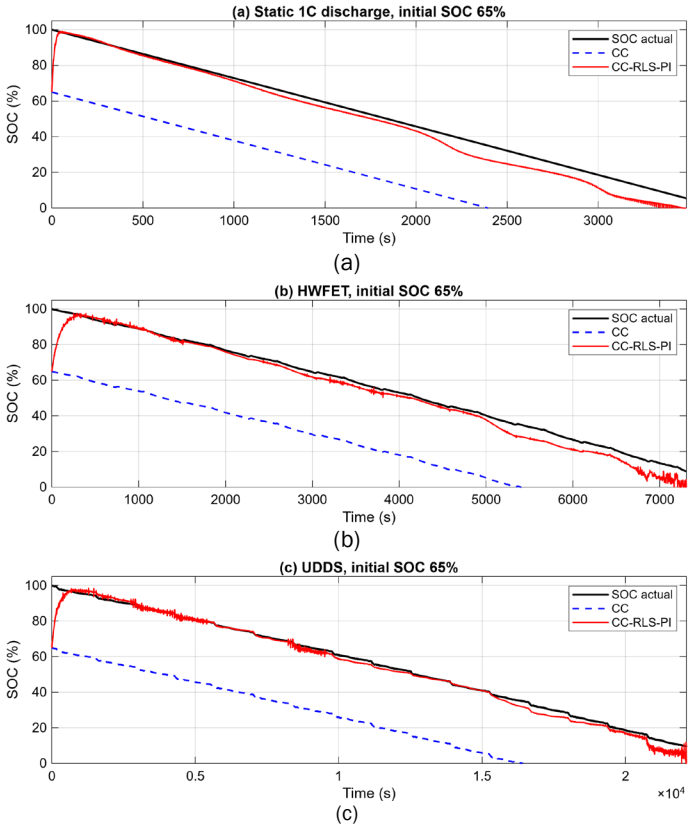


Figure 5. SOC estimates of the actual SOC, CC and CC-RLS-PI for Scenario C (assumed initial SOC 65%): (a) static 1C, (b) HWFET, (c) UDDS.

Entry is not settling. In none of the nine runs does the error stay inside ±2% until the true SOC falls below 30%; the estimate is inside the band for 40.5–41.7% (static), 57.9–62.0% (HWFET) and 81.5–84.2% (UDDS) of that time and leaves it again (Figure 6). Looser bands are met sooner: after 0–245 s the error stays below 10 points until SOC < 30% (t_{10} in Table 3). After first entry, the largest error is 9.8, 11.4 and 10.2 points on the static, HWFET and UDDS profiles, independent of the scenario, and it occurs at low SOC (Table 4). The hybrid estimator therefore removes the initial offset but leaves an error of the order of the band, and “converged” should not be read as “accurate within 2%”.

Table 3. Recovery metrics of the hybrid estimator. t_1: first entry into ±2%; in band: share of samples within ±2% before SOC < 30%; t_{10}: time after which the error stays within ±10% until SOC < 30%.

Load profile	Scenario	RMSE (%)	t_1 (s)	In band (%)	t_{10} (s)
Static 1C	A	4.766	1	41.7	0
	B	4.837	24	40.9	8
	C	5.008	30	40.5	16
HWFET	A	3.746	9	62.0	0
	B	4.050	175	59.0	63
	C	4.669	244	57.9	121
UDDS	A	2.022	5	84.2	0
	B	2.361	344	82.1	116
	C	3.015	389	81.5	245

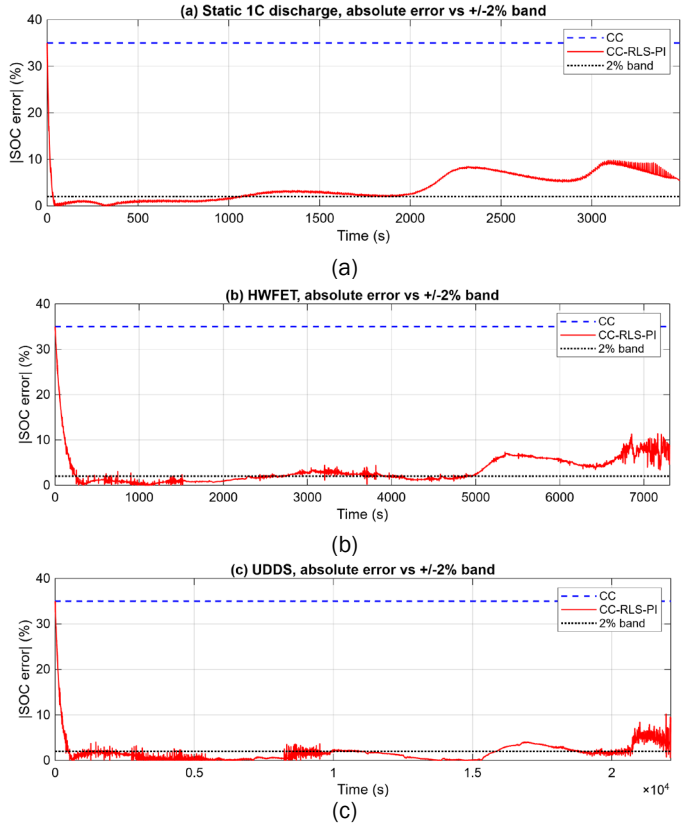


Figure 6. Absolute SOC error of CC and CC-RLS-PI against the ±2% band for Scenario C: (a) static 1C, (b) HWFET, (c) UDDS.

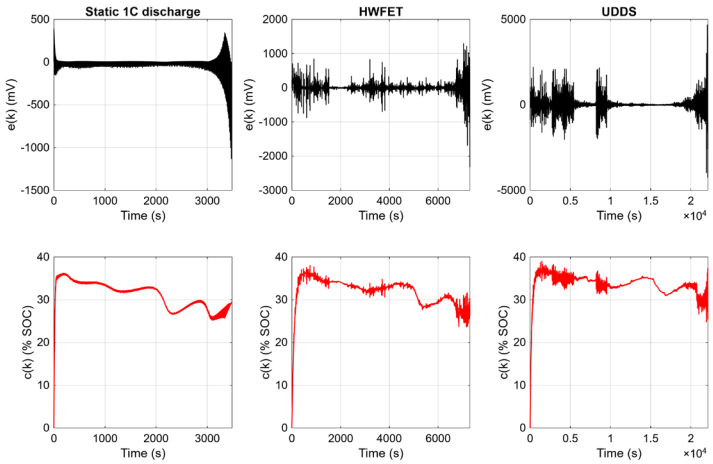


Figure 7. OCV residual *e(k)* (top) and correction *c(k)* (bottom) for Scenario C: static 1C, HWFET and UDDS (left to right).

3.3 Accuracy by SOC Range

Table 4 splits the error after first entry by SOC range (Scenario C). Above 40% SOC the MAE stays between 0.75 and 3.0 points on all three profiles, but below 40% it rises to 5.0–7.7 points on the static and HWFET profiles and 2.4–3.5 points on UDDS; the MAE restricted to SOC < 30% is 6.9, 6.1 and 3.0 points for the static, HWFET and UDDS profiles. Two mechanisms limit the accuracy there. First, the OCV slope is small near 37% SOC (0.315 V per unit SOC), so a 10 mV OCV error equals 3.2 points of SOC. Second, errors in V_t from the fixed-parameter model are amplified about 22 times in (14). Both are consistent with the pattern, but neither was isolated experimentally, and a mismatch of the single RC branch at low SOC cannot be excluded (the large scatter of R_p and C_p below 30% SOC in Figure 1b points the same way). Lowering this error would require SOC-dependent parameters or a second RC branch.

Table 4. MAE (points of SOC) by true SOC range (%) after first entry, Scenario C, and the maximum error after first entry (points).

Load profile	100–80	80–60	60–40	40–30	30–20	20–0	Max error
Static 1C	0.78	2.14	3.00	7.74	5.81	7.68	9.8
HWFET	0.75	2.01	1.87	5.75	4.98	7.21	11.4
UDDS	0.94	0.85	0.90	2.74	2.39	3.52	10.2

3.4 When the Correction Helps

Because CC with a correct start is exact here and the hybrid MAE stays between 1.5 and 4.0% whatever the initial error, there is a break-even initial error below which plain CC is better. Over the tested values, the hybrid MAE falls below the CC MAE only from $|e_{init}| = 4$ points on the static profile (3.867 against 4.000), 3 points on HWFET (2.930 against 3.004) and 2 points on UDDS (1.513 against 1.999). For an initial error of 1 point, CC gives about 1.0 while the hybrid gives 3.9, 2.9 and 1.5 on the three profiles. The hybrid estimator also recovers from positive errors: starting at a true SOC of 60% with assumed values 2, 20 and 35 points too high, its MAE is 5.6–5.8 (static), 4.2–4.9 (HWFET) and 2.0–2.5 (UDDS), against 2, 20 and 35 for CC.

When the cell is fully charged and rested, as at the start of the HWFET and UDDS files, the OCV from the rest voltage (or from $V_t + IR_0$) gives an essentially exact initial SOC and CC then has an MAE of 0.004–0.005%, far below any hybrid result. This is the most favorable case for OCV initialization, since the true SOC is 100% by construction. The static profile starts under load, so no rest voltage exists: the loaded voltage gives an error of 10.3 points, and 1.34 points with IR compensation. The meaningful test is a start at mid-SOC under load (Table 5). There, the hybrid MAE is lower than that of IR-compensated OCV initialization in 7 of 9 cases and lower than that of the raw loaded voltage in 8 of 9. It loses to the IR-compensated value at HWFET and UDDS from 80% SOC (3.85 against 3.77 and 1.91 against 1.24) and to the raw voltage at UDDS from 60% (2.23 against 1.29). The advantage grows as the start SOC decreases (OCV-init error of 9.7–15.9 points against a hybrid MAE of 3.3–7.0 at 40%), which is consistent with the smaller OCV slope and larger voltage drops at low SOC, although this was not isolated. In these runs the hybrid estimator began from a +20 point error to stand in for an unknown start, whereas the OCV initialization errors are set by the voltage.

Table 5. MAE (%) for starts at mid-SOC under load without rest; bold marks the lowest value per row. The hybrid estimator started with a +20 point error.

Load profile	True SOC at start (%)	OCV-init, $V+IR_0$	OCV-init, raw V	CC-RLS-PI
Static 1C	80	8.88	19.36	4.76
	60	8.89	23.11	5.68
	40	15.95	22.85	6.96
HWFET	80	3.77	8.54	3.85
	60	6.03	10.88	4.51
	40	12.86	18.57	5.90
UDDS	80	1.24	1.98	1.91
	60	2.95	1.29	2.23
	40	9.66	21.27	3.31

3.5 Sensitivity to the Gains and the Forgetting Factor

Table 6 summarizes the gain grid of Section 2.5. Between 12 and 18 of the 36 pairs per profile are feasible, and the gains used here are all inside the feasible region. Inside it, speed and smoothness conflict: on the static profile the fastest feasible pair (0.02, 0.1 s) enters the band in 8 s but with a correction noise of 1.30 points/s, whereas the pair used needs 30 s with 0.24 points/s; the feasible first-entry times span 67–704 s on HWFET and 96–1265 s on UDDS. A single gain also works: applying the HWFET gains (0.02, 2 s) to all profiles changes the MAE by at most +0.5 points relative to per-profile gains (static C: 4.478 against 3.981; UDDS: 1.58–1.70 against 1.51–1.76), whereas the static gains on UDDS give a maximum error of 39.3 points, above the 35-point initial offset, because the correction follows the noisy OCV residual. A per-profile gain is therefore not required, but the gain of the static profile should not be used for dynamic loads.

Table 6. Gain feasibility on the 6 × 6 grid (Scenario C metrics) and the gains used. Noise: standard deviation of the per-second change of *c(k)* after first entry.

Load profile	Feasible pairs	MAE range (%)	t_1 range (s)	Used K_p, T_i (s)	t_1 (s)	MAE (%)	Noise (pt/s)
Static 1C	18 of 36	3.89–4.49	8–307	0.002, 0.03	30	3.98	0.24
HWFET	14 of 36	3.11–3.78	67–704	0.02, 2	244	3.31	0.38
UDDS	12 of 36	1.63–1.97	96–1265	0.01, 2	389	1.76	0.42

Table 7 shows the effect of the forgetting factor. Changing λ moves the identified R_p from 0.022 to 0.074 Ω and C_p from 876 to 1020 F, while R_0 and the voltage fit error (16–17 mV) hardly change, so the identification data do not discriminate between these R_p values. The SOC error does: the MAE of Scenario B on the static profile ranges from 2.68 to 10.1% (HWFET 2.15–4.42%, UDDS 1.48–1.88%). The value λ = 0.985 of the original analysis is not the one giving the lowest MAE (λ = 0.99 is), and it is reported unchanged instead of selecting λ on the estimation error. The accuracy figures of this paper should therefore be read with an uncertainty of several points set by R_p.

Table 7. Effect of the RLS forgetting factor on the identified parameters and on the hybrid MAE (R_0 stays at 0.0301 Ω).

λ	R_p (Ω)	C_p (F)	Voltage MAE (mV)	MAE static	MAE HWFET	MAE UDDS
0.982	0.0222	876	16.9	4.39	3.32	1.68
0.985	0.0242	887	16.9	3.90	3.11	1.63
0.990	0.0356	900	17.0	2.68	2.15	1.48
0.995	0.0737	914	17.1	10.12	4.42	1.88
0.999	0.0686	1020	15.9	8.85	3.81	1.76

3.6 Comparison with Kustiman et al.

Table 8 sets the results against [19], which used the same three initial values. The MAE reported there (0.405, 0.498 and 0.591%) is lower than ours by factors of about 6–10 on the static and HWFET profiles and 3–4 on UDDS. The two studies are not directly comparable: [19] used a 260 mAh cell on its own hardware under a pulsed 260 mA load that includes 30 s without load, with its own gains and parameter identification, whereas we use a 2.9 Ah cell with public drive-cycle data, continuous load and fixed offline parameters. The present data cannot tell which of these differences explains the gap; the sensitivity to R_p (Table 7) and the OCV-slope argument of Section 3.3 show that part of it can be set by the parameters and the OCV fit alone. Our results therefore support the recovery capability reported in [19], but they place the accuracy under standard dynamic profiles at an MAE of 1.5–4.0%, not at the level reported there.

Table 8. Comparison with Kustiman et al. [19].

Item	Kustiman et al. [19]	This study
Cell	260 mAh, 3.7 V, own hardware	Panasonic 18650PF, 2.9 Ah, public data
Load	Pulsed 260 mA, 20 s on, 30 s off	Static 1C; HWFET; UDDS (continuous)
PI gains	K_p = 0.05, T_i = 0.02 s (Ziegler–Nichols and trial)	K_p = 0.002–0.02, T_i = 0.03–2 s (per profile)
MAE, A/B/C (%)	0.405 / 0.498 / 0.591	Static 3.864/3.920/3.981; HWFET 2.924/3.117/3.309; UDDS 1.513/1.634/1.760
Convergence	About 200 s (B and C)	First entry into ±2%: 1–389 s; never settles in ±2%

3.7 Computational Load

The comparison is made by operation count, which does not depend on the host. Per sample, CC needs one multiplication and one addition. The hybrid estimator adds the OCV reconstruction (14) (4 multiplications and 3 additions with precomputed coefficients), the 9th-degree polynomial in Horner form (9 and 9), the PI law (16) (2 and 2) and a few additions and comparisons for (15) and (17), about 16 multiplications and 18 additions in total. Because RLS runs offline, no matrix operation is performed in the loop; running a 3 × 3 RLS online would add a cost that was not evaluated here. Execution times measured in MATLAB on a laptop are not reported, because they mainly reflect the interpreter and not the algorithm; execution on embedded hardware is left for future work.

3.8 Limitations

Six limitations bound the conclusions. First, no noise or sensor bias was injected, and the dataset carries laboratory-grade current measurement, so the drift term of (2) is negligible here. For orientation, a persistent bias of 0.5%, 1% and 2% of a 20 A full-scale sensor integrates to 3.37, 6.74 and 13.48 points of SOC in one hour on this 2.9677 Ah cell, which is of the order of the initial errors studied; whether the hybrid estimator suppresses this component is untested.

Second, the reference SOC is the CC integral of the same current, so CC with a correct start is exact by construction; the tests cannot reveal CC drift, and the break-even result is conditional on this. Third, the RLS parameters were identified offline on the same cell and temperature and held fixed; online RLS, SOC- or temperature-dependent parameters and ageing were not examined, and the outcome depends strongly on R_p (Table 7). Fourth, all tests used a single cell at 25 °C; cell-to-cell variation was not examined.

Fifth, the feasibility thresholds of Section 2.5, the 20-point initial error of the mid-profile starts and the choice of the ±2% band are choices of the authors. Sixth, no comparison with EKF-type filters was made, so nothing is claimed about the relative accuracy or efficiency of the two families.

4 Conclusion

This study evaluated the CC-RLS-PI scheme of [19] on a Panasonic 18650PF cell under static 1C, HWFET and UDDS profiles with offline-identified, fixed parameters. First, the hybrid estimator removes a large initial SOC error: it first entered the ±2% band after 1–389 s from initial errors of 2–35 points, but its error did not stay within 2 points in any run, and its MAE of 1.5–4.0% rose to 5.0–7.7 points below 40% SOC on the static and HWFET profiles. Second, the correction has a break-even: plain CC is more accurate when the initial error is below about 4, 3 and 2 points on the static, HWFET and UDDS profiles.

Third, against OCV initialization, the hybrid estimator gave the lower MAE in 7 of 9 starts at mid-SOC under load without rest, but OCV initialization from a rest voltage is far more accurate when a rest period exists. Fourth, the outcome depends on the identified R_p (MAE of 2.7–10% on the static profile for λ from 0.982 to 0.999), and compared with [19] the MAE under standard profiles is several times higher. The scheme is therefore suited to recovery from large initial errors when OCV initialization is unreliable, within an accuracy limit of about 2–4 points. Further work is a current-noise injection study, online identification, a comparison with EKF-type filters, and execution on embedded hardware.

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